PERUN
Technologies

LARA-100 MOTHERBOARD

USER MANUAL

CONTENTS

1 FIRST THINGS FIRST: LARA-100 PLATFORM

Before we give detailed information about LARA-100 Motherboard, let us make a brief introduction in LARA-100 system in order to get a bigger scope.

If you have been already familiar with LARA-100 concepts **you can skip this first chapter and go immediately to the second**.

1.1 WHY LARA-100?

The vision behind LARA-100 is to serve its users as a sort of a LAunch RAmp for Power Electronics project development, research and education. It emerged as the comprehensive answer to the permanent need for flexibility and comfortable performance in the PE laboratory.

So, how LARA-100 serves you? Instead of building and maintaining a new test-bench whenever dealing with a new project or application, PERUN brings you the LARA-100 platform which can be re-configured and re-used according to your present requirements.

Therefore, LARA-100 is designed to solve the following:

1. It replaces standard inflexible laboratory test benches and their exhausting modifications with the platform which can be configured to cover a variety of applications (motor drives, active filters, PV converter, FACTS, as well as to support some larger research projects, e.g. micro-grids and smart grids).
2. LARA-100 interfaces with popular controllers such as Texas Instruments C2000 series following the simple plug and play principle
3. User's control algorithm is tested directly from an intuitive software suite called PERUN Power Desk (PPD) which facilitates:
    - Embedded oscilloscope function which reduces the need for the external oscilloscope
    - Supervisory control over the system operation
    - Tag Explorer with the on-line access (read and write) to all variables and parameters defined by a user
    - Signal Analysis Desk which processes and analyzes measured results and
    - Control Design Desk which helps user to design the new control algorithm or modify the existing one
    - Test automation through scripting functionality

1.2 WHAT IS LARA-100?

The idea behind LARA-100 is very simple and it can be summarized as follows (Figure 1): let us assemble our power electronics based system using puzzle-like components: configurable power stage, extension boards, controller and software. Different combinations of "puzzles" make possible simple

configuration and re-configuration of the same setup in the system we need at a time (motor drive, active filter, PV converter, STATCOM….

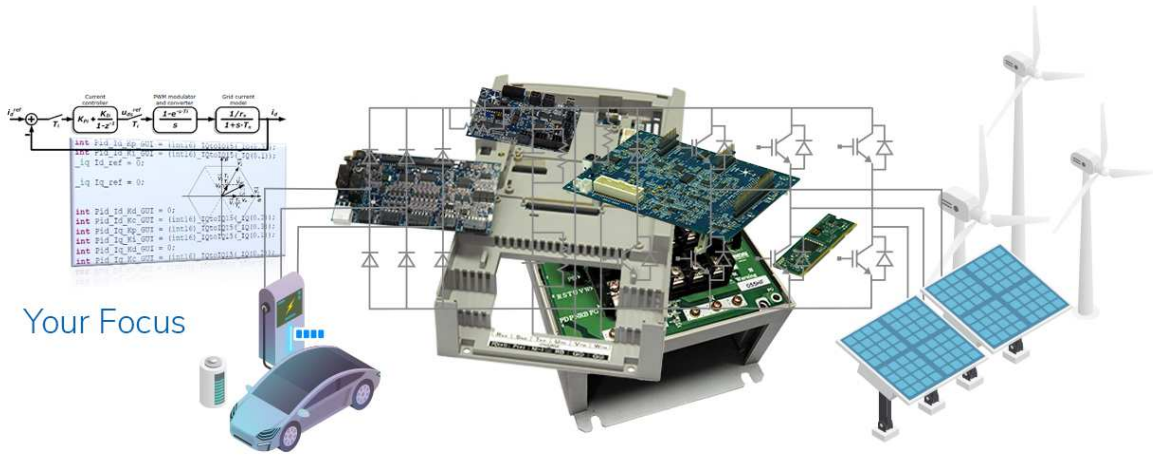


Figure 1: LARA-100K concept - reconfigurable platform to support applications in your focus

LARA-100K platform consists of

- ***LARA Power Stage***
- ***LARA Expansion Boards*** and
- ***PERUN PowerDesk*** software suite.

LARA Power Stage can be configured into different topologies such as single and three phase rectifier, single and three-phase inverter, boost, interleaved boost (up to 4 phases) and choppers. LARA Power Stage can be controlled with switching frequency up to 100 kHz (hence the name 100K). The LARA power range is up to 5.5 kW, but can be extended on request.

The role of LARA's Expansion Boards together with the PERUN PowerDesk software suite is crucial in the concept of LARA-100 as the open and configurable platform. The role of Expansion Boards is:

- interfacing with popular controllers such as Texas Instruments C2000 series
- expanding the scope of possible LARA's applications (motor drives, renewables, automotives, etc.)
- communication with variety of external devices such as encoders, resolvers, PLCs, other LARAs, etc. through CAN, USB, Ethernet, JTAG and RS485.

LARA-100 Expansion Boards are:

- *LARA-100 Motherboard* as the main component together with -
- Application Boards
- Communication and
- GPIO Boards.

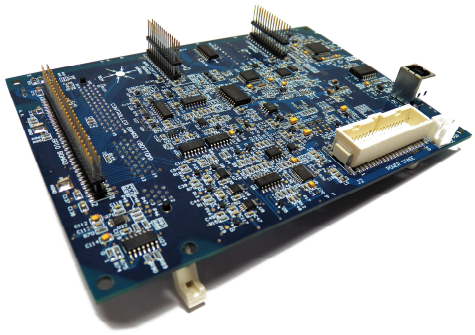


Figure 2: LARA-100 Motherboard

LARA-100 Motherboard has two main functions: the first one is to enable easy plug-in of controllers (Texas Instruments C2000 series) and the second one is to host other Expansion boards based on plug-in principle. You might think of it in similar way as of PC motherboard.

The role of ***LARA-100 Application Boards*** (APP Boards) is to extend the LARA-100 system functionalities and features related to specific power electronics applications. There are two main types of Application boards: Motor drive and Grid-Connected. The first one enables direct interfacing with incremental/absolute encoders, resolvers or tachogenerators. The second one supports interfaces with grid voltage lines, photovoltaic (PV) strings, currents measurements, etc. i.e. supports grid-connected applications.

LARA-100 Communication Boards or simply COMM Boards are compact boards for extension of LARA-100 system with a variety of standard communication interfaces such as *Ethernet*, *CAN* or *RS-485* communication buses. Application note: COMM Boards are ideal solution to form complex systems such as micro- and smart-grids, where COMMs are connected with supervisory controllers and several LARAs that stand for different grid elements.

LARA-100 GPIO (General Purpose Input/Output) comes with all sorts of digital and analog input and output circuitries. Suitable GPIO Board directly interfaces switches, buttons, power relays, power contactors, power LEDs, meters, or industrial PLCs with LARA-100 system controller and quickly build power electronics hardware platform immediately ready for control development and testing.

LARA's software suite *PERUN PowerDesk* is responsible for

- system configuration
- supervisory control
- data acquisition
- real time access to all controller variables
- analysis of measured signals (real time filtering, Fourier)
- mathematical manipulations over signals in real time
- control design tools (Bode plots, etc.)
- scripting and test automation

PERUN PowerDesk can be utilized as an integral part of LARA-100 system as described above, but also it can be employed as a **standalone** software package. In this scenario a user can develop and test a control code on Texas Instruments C2000 controller using Perun PowerDesk for all mentioned purposes except for system configuration (since there is no LARA's hardware). What do you need in this case? Clearly you need a docking board to plug in controller and a PC with installed PERUN PowerDesk. You can use either LARA-100 Motherboard or TI's Experimenter's kit in the role of the docking board.

Automatic code generation (auto-coding) from ***Matlab Simulink*** is supported in PERUN PowerDesk which makes the process of control design much easier and comfortable. Simply, auto-coding is here to generate the designed algorithm and PERUN PowerDesk tools proceed with evaluation, testing and re-design.

LARA-100 with its HW and SW components presents well rounded and open re-configurable platform (Figure 3).

Frequently asked questions related to PERUN PowerDesk software suite:

Can I use PERUN PowerDesk without LARA-100 hardware?

The answer is yes. You can use PPD in a standalone version. In that case you can test and debug your control code for any kind of application. All you need is Texas Instruments C2000 DSP, a PC with installed PERUN PowerDesk, a docking board for DSP such as TI's Experimenter Kit or LARA's Motherboard

Can I write a control code directly from PERUN PowerDesk?

The answer is no. The writing of control code is performed with the tool which provides controller manufacturer, for instance Code Composer Studio if you use Texas Instruments Controller. The role of PERUN PowerDesk is to assist you in Comfortable higher level debugging and testing through Tag Explorer, Oscilloscope function and real time signal manipulations and analysis.

What is the difference between PPD Standalone and version which comes with LARA-100?

Both versions have the same key features (PERUN Tag Explorer, Oscilloscope and Signal Analysis Desk. The version which comes with LARA has a link to LARA HW and therefore enables supervisory control of LARA configured in one of required Power Electronics applications.

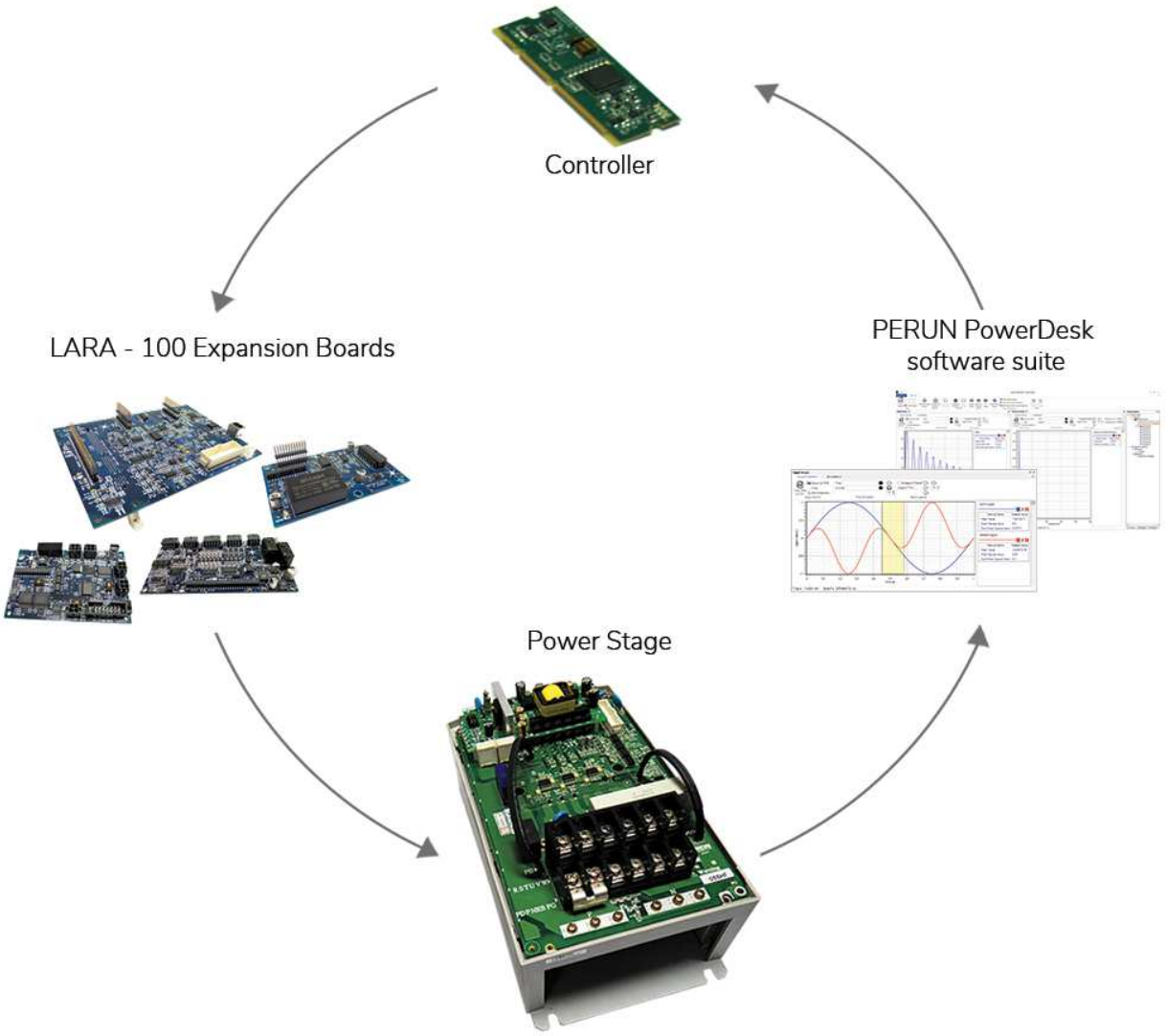


Figure 3: LARA-100 main components

In the continuation of this document the focus is set to ***LARA-100 Motherboard***.

2 LARA 100 MOTHERBOARD

LARA-100 MOTHERBOARD is a main board interfacing power electronics stage (LARA Power Stage) and its controller (Controller Board). Making and putting together fully-functional power electronics devices opened for control development and testing, have never been easier!

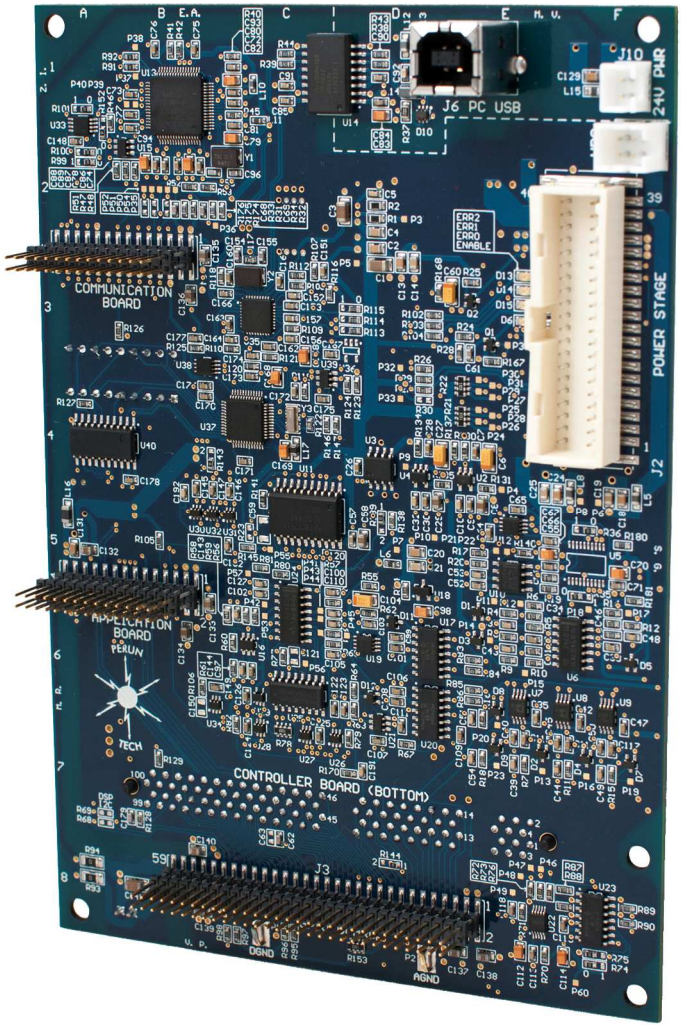


Figure 4: LARA 100 Motherboard

Figure 5 and Figure 6 gives overview of external connection interfaces.

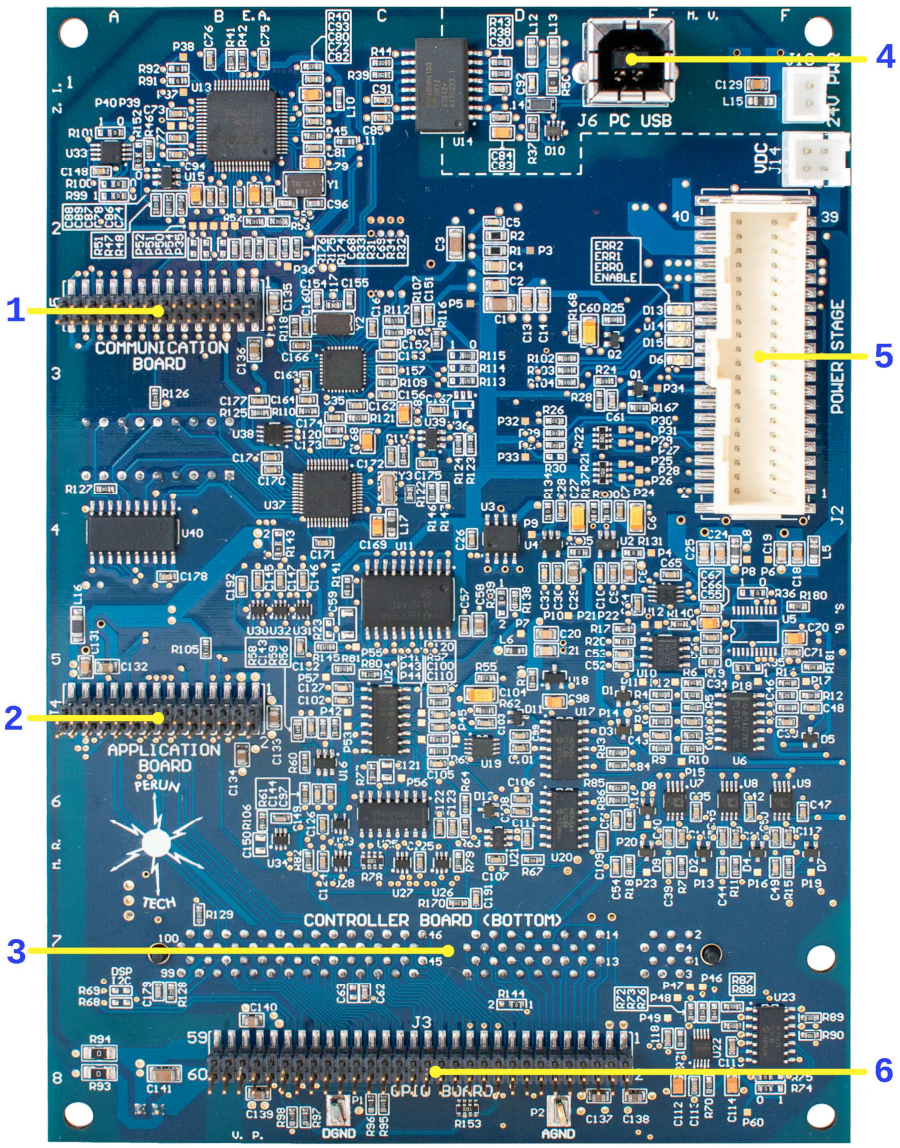


Figure 5: LARA 100 Motherboard connectors – upper side

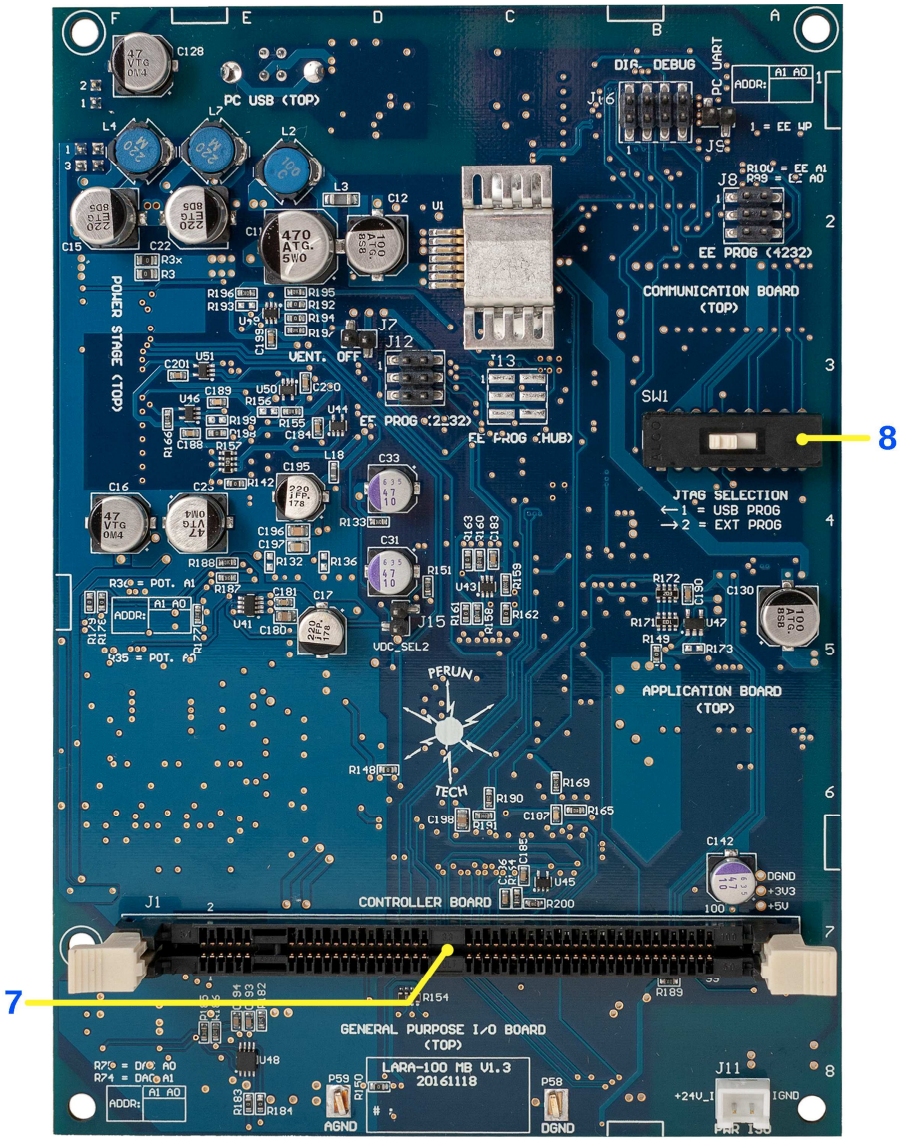


Figure 6: LARA 100 Motherboard connectors – bottom side

Connectors have the following meaning:

1 – **Communication Board interface –** Connect supervisory and power stage controller over different communication buses, such as RS-232, RS-485, CAN or Ethernet, with just plugging suitable PERUN's Communication Board.

2 – **Application Board interface –** Adapt the LARA-100 system to the specific power electronics application, using one of the PERUN's Application Boards. Go ahead and work with motor drives, grid-connected converters or solar boost converters right away.

3 – **Controller Board interface (on bottom side) –** See note 7.

4 – **USB interface –** Configure, monitor and control your power electronics device through PERUN's PowerDesk software suite.

5 – **Power Stage interface –** Interface all control, feedback and protection signals of power stage in appropriate and safe manner with your controller.

6 – **GPIO Board interface –** Take advantage of PERUN's GPIO Boards, and expand functionality of your power electronics device through different digital and analog inputs and outputs.

7 – **Controller Board interface –** LARA-100 Motherboard has DIMM100 socket for connecting the power stage controller. This makes it plug-and-play compatible with wide range of Texas Instruments C2000 control cards. Just plug TMS320F28335 controlCARD, upload appropriate PERUN's example code and you are ready to control your power stage.

8 – **JTAG selection switch –** Select between on-board XDS100 JTAG programmer / debugger or external programmer / debugger connected to the corresponding connector on PERUN's Communication Board.

LARA-100 Motherboard is plug-and-play solution compatible with all Texas Instruments industry-standard DIMM100 controlCards, such as TMDSCNCD28335 with TMS320F28335 high-performance floating-point controller that operates at 150 MHz, has 256K x 16-bits Flash, 34K x 16-bits SRAM, and I/O peripherals optimized for power electronics applications. Having sockets for Power Stage, Application, GPIO and Communication Boards, LARA-100 Motherboard utilizes all of the controller's peripheral I/Os important for LARA-100 power electronics system control. This makes LARA-100 system easy adaptable to various power electronics applications and different supervisory controllers. Motherboard functionalities can be extended by using various PERUN's Application, GPIO and Communication Boards. FIGURE 6 gives an overview of connections between TI DIMM100 Control Cards and Motherboard's main connectors.

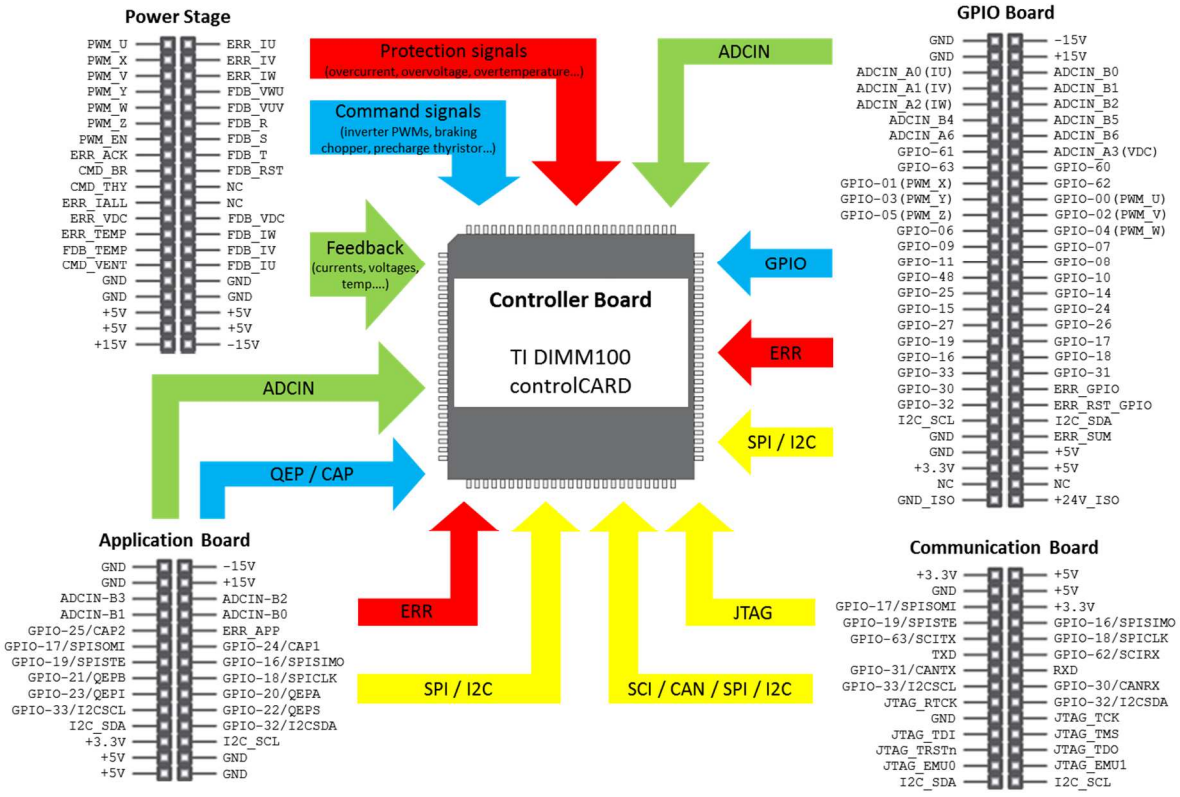


Figure 7: Pinout of LARA 100 Motherboard connectors and overview of controller connections

Controller on-board JTAG programmer/debugger

To make your control prototyping experience as convenient as possible, LARA-100 Motherboard has built-in XDS100 v1 JTAG programmer/debugger. User can use standard programming/debugging environment, such as Texas Instruments Code Composer Studio, or directly program and debug his controller with PERUN PowerDesk software. He just needs to connect Motherboard with dedicated USB link to the programming environment and he is ready to upload control code. Optionally, desired external JTAG programmer/debugger can be used by connecting it to the controller through our Communication Boards. Motherboard's USB/JTAG interface, and moreover JTAG interface on Communication Boards, are galvanically isolated from user's programming/debugging device.

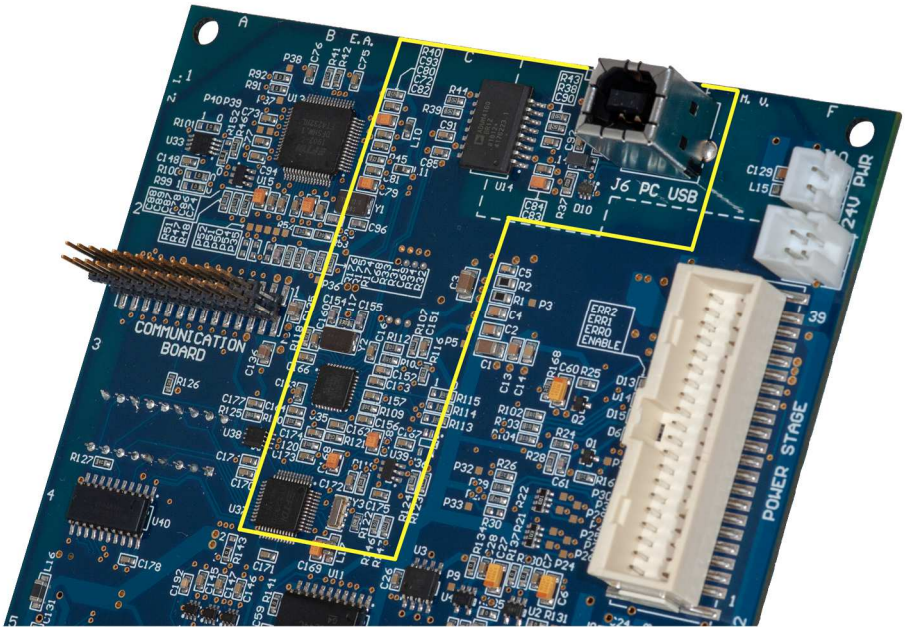


Figure 8: Controller on-board JTAG programmer/debugger interface

Control code debugging

By using PERUN PowerDesk software user can efficiently eradicate mistakes and iron out control code in various applications, such as motor drive, PV boost converter or grid-connected converter in order to work according to set requirements. It's project-organized easy-to-use software environment used for configuration, monitoring and high-level control of whole LARA-100 system. It's special features are Scope function allowing user to monitor any of controller's real-time variables and Tag Explorer for setting control variables and parameters reference values, turning the PERUN PowerDesk into ideal platform for high-level debugging of power electronics applications. Motherboard's USB/UART debugging interface is galvanically isolated from user's programming/debugging device (PC with PERUN PowerDesk software). Moreover, you can use PERUN PowerDesk for control code high-level debugging of any embedded microcontroller system with integrated USB/UART bridge.

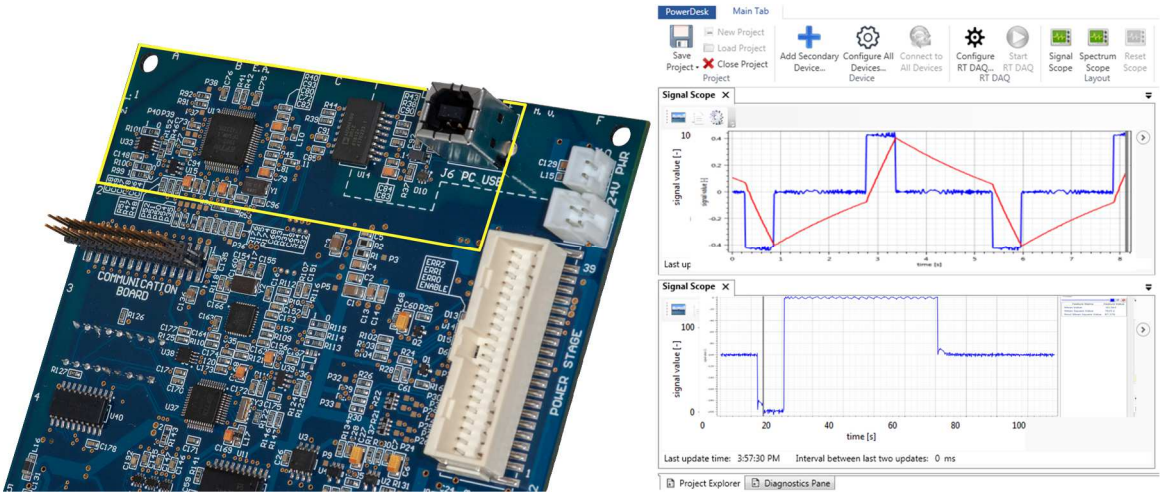


Figure 9: Control code debugging

Technical specification for Motherboard

LARA Motherboard provides industrial-grade compactness to the overall LARA-100K platform. There is no need for multitude of long wires connecting the controller and power stage units, controller is nicely packed locally where the power stage is, making the whole LARA-100K system much less sensitive to signal noise typical for power electronics devices switching nature. In that way, complete LARA-100K system have external layout as industrial drives, which is not usual case with open development platforms.

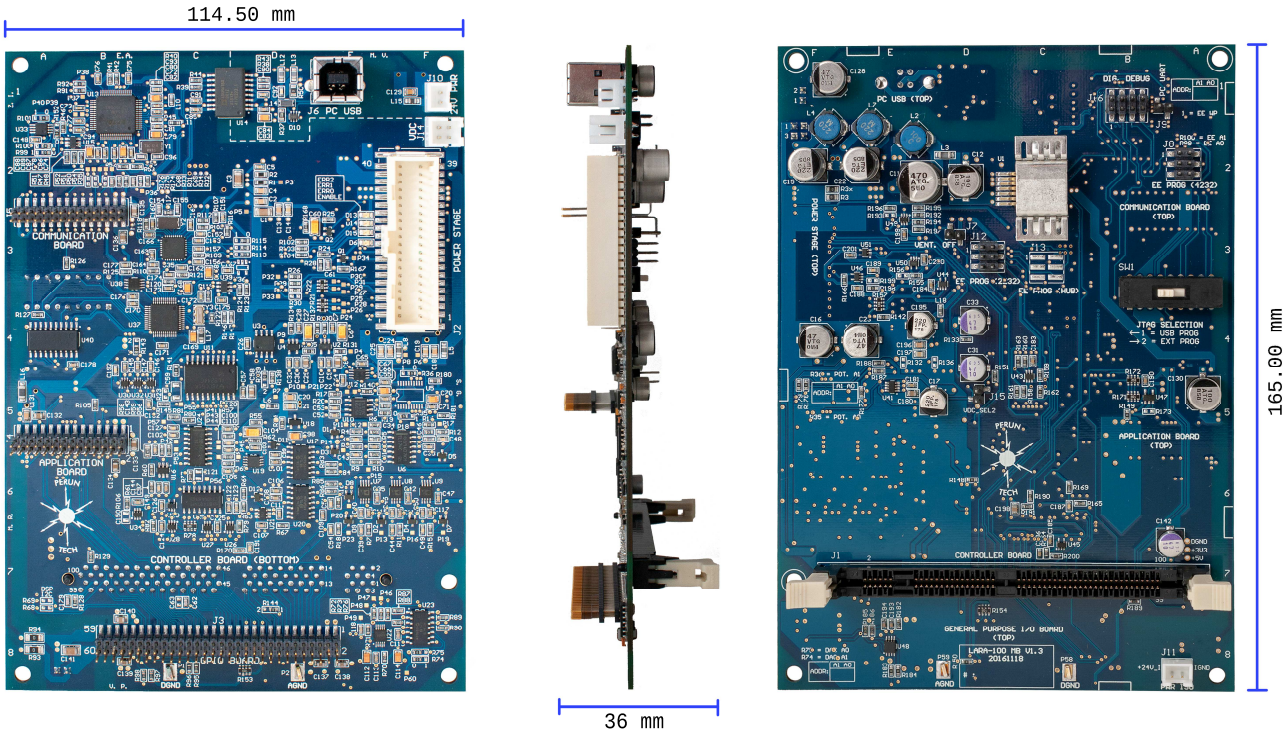


Figure 10: LARA 100 Motherboard dimensions

Motherboard's top side connectors are properly aligned with cover box holes, and at the bottom side there is a connector (J1) for Controller Board.

Connections – Controller Board (J1)

LARA-100 Motherboard has DIMM100 connector (TE Connectivity part number 5390213-1, standard MO-161) for direct use with compatible Texas Instruments controlCARDs or custom made Controller Boards. It is placed on the bottom side of Motherboard, in the slot shown in Figure 11.

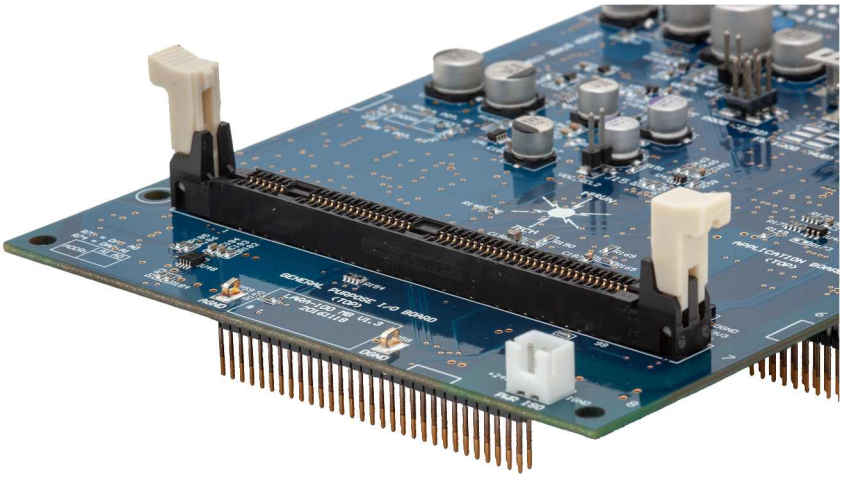


Figure 11: Controller board connector (J1)

A pin assignment of controller board connector is given in following table:

Table 1: Pin assignment of controller board interface (J1)

Pin	Signal	Description
1	N.C.	Not used
2	N.C.	Not used
3	N.C.	Not used
4	N.C.	Not used
5	N.C.	Not used
6	N.C.	Not used
7	N.C.	Not used
8	N.C.	Not used
9	N.C.	Not used
10	N.C.	Not used
11	N.C.	Not used
12	N.C.	Not used
13	ADCIN-B0	Controller analog input B0
14	DSP_IU/ADCIN-A0	Measured inverter line current IU
15	GND	Electronics ground reference
16	GND	Electronics ground reference

Pin	Signal	Description
17	ADCIN-B1	Controller analog input B1
18	DSP_IV/ADCIN-A1	Measured inverter line current IV
19	GND	Electronics ground reference
20	GND	Electronics ground reference
21	ADCIN-B2	Controller analog input B2
22	DSP_IW/ADCIN-A2	Measured inverter line current IW
23	GND	Electronics ground reference
24	GND	Electronics ground reference
25	ADCIN-B3	Controller analog input B3
26	DSP_VDC/ADCIN-A3	Measured DC-link voltage
27	GND	Electronics ground reference
28	GND	Electronics ground reference
29	ADCIN-B4	Controller analog input B4
30	DSP_TEMP/ADCIN-A4	Measured heatsink temperature
31	N.C.	Not used
32	N.C.	Not used
33	ADCIN-B5	Controller analog input B5
34	VREF/ADCIN-A5	Reference offset voltage (for currents)
35	PPD_RST/GPIO-58	Reset PERUN PowerDesk (PPD) scope
36	ERR_RST_DSP/GPIO-59	Error reset/acknowledgment
37	ADCIN-B6	Controller analog input B6
38	ADCIN-A6	Controller analog input A6
39	GPIO-60	Controller general purpose input/output 60
40	GPIO-61	Controller general purpose input/output 61
41	ADCIN-B7	Controller analog input B7
42	ERR_CODE/ADCIN-A7	Error code in analog format
43	GPIO-62/SCIRX-C	Controller GPIO or SCI pin [1)]
44	GPIO-63/SCITX-C	Controller GPIO or SCI pin [1)]
45	DSP_GU/GPIO-00/EPWM-1A	PWM signal for upper switch phase U

Pin	Signal	Description
46	DSP_GX/GPIO-01/EPWM-1B	PWM signal for lower switch phase U
47	DSP_GV/GPIO-02/EPWM-2A	PWM signal for upper switch phase V
48	DSP_GY/GPIO-03/EPWM-2B	PWM signal for lower switch phase V
49	DSP_GW/GPIO-04/EPWM-3A	PWM signal for upper switch phase W
50	DSP_GZ/GPIO-05/EPWM-3B	PWM signal for lower switch phase W
51	GPIO-06/EPWM-4A	Controller GPIO or PWM pin [1)]
52	GPIO-07/EPWM-4B/ECAP-2	Controller GPIO or PWM or CAP pin [1)]
53	GND	Electronics ground reference
54	+5V	Power supply +5V for Controller Board
55	GPIO-08/EPWM-5A	Controller GPIO or PWM pin [1)]
56	GPIO-09/EPWM-5B/ECAP-3	Controller GPIO or PWM or CAP pin [1)]
57	GPIO-10/EPWM-6A	Controller GPIO or PWM pin [1)]
58	GPIO-11/EPWM-6B/ECAP-4	Controller GPIO or PWM or CAP pin [1)]
59	DSP_VUV/GPIO-48/ECAP-5	Measured inverter output voltage VUV
60	PWM_EN/GPIO-49	PWM enable signal
61	N.C.	Not used
62	N.C.	Not used
63	N.C.	Not used
64	+5V	Power supply +5V for Controller Board
65	ERR/GPIO-12/TZ-1	Error signal (indicating error state) [1)]
66	ERR_DSP/GPIO-13	Controller error triggering signal
67	GPIO-15/TZ-4/SCIRX-B	Controller GPIO or TZ or SCI pin [1)]
68	GPIO-14/TZ-3/SCITX-B	Controller GPIO or TZ or SCI pin [1)]
69	GPIO-24/ECAP-	Controller GPIO or CAP or QEP pin [1)]

Pin	Signal	Description
	1/EQEPA-2	
70	GPIO-25/ECAP-2/EQEPB-2	Controller GPIO or CAP or QEP pin [1)]
71	GPIO-26/ECAP-3/EQEPI-2	Controller GPIO or CAP or QEP pin [1)]
72	GPIO-27/ECAP-4/EQEPS-2	Controller GPIO or CAP or QEP pin [1)]
73	GND	Electronics ground reference
74	+5V	Power supply +5V for Controller Board
75	GPIO-16/SPISIMO-A/CANTX-B	Controller GPIO or SPI or CAN pin [1)]
76	GPIO-17/SPISOMI-A/CANRX-B	Controller GPIO or SPI or CAN pin [1)]
77	GPIO-18/SPICLK-A/SCITX-B	Controller GPIO or SPI or SCI pin [1)]
78	GPIO-19/SPISTE-A/SCIRX-B	Controller GPIO or SPI or SCI pin
79	GPIO-20/EQEPA-1/CANTX-B	Controller GPIO or QEP or CAN pin [1)]
80	GPIO-21/EQEPB-1/CANRX-B	Controller GPIO or QEP or CAN pin [1)]
81	GPIO-22/EQEPS-1/SCITX-B	Controller GPIO or QEP or SCI pin [1)]
82	GPIO-23/EQEPI-1/SCIRX-B	Controller GPIO or QEP or SCI pin [1)]
83	N.C.	Not used
84	+5V	Power supply +5V for Controller Board
85	RXD_PPD/GPIO-28	Serial receive data pin reserved for PPD
86	TXD_PPD/GPIO-29	Serial transmit data pin reserved for PPD
87	GPIO-30/CANRX-A	Controller GPIO or CAN pin [1)]
88	GPIO-31/CANTX-A	Controller GPIO or CAN pin [1)]
89	GPIO-32/I2CSDA	Controller GPIO or I2C pin [1)]
90	GPIO-33/I2CSCL	Controller GPIO or I2C pin [1)]

Pin	Signal	Description
91	DSP_BR/GPIO-34	Braking chopper ON/OFF signal
92	+5V	Power supply +5V for Controller Board
93	GND	Electronics ground reference
94	TDI	Controller JTAG test data input TDI
95	TCK	Controller JTAG test clock input TCK
96	TDO	Controller JTAG test data output pin
97	TMS	Controller JTAG test mode signal TMS
98	TRSTn	Controller JTAG test reset signal
99	EMU1	Controller JTAG emulator input EMU1
100	EMU0	Controller JTAG emulator input EMU0

[1)] For full utilization of PERUN's LARA-100 system functions and features (with expansion boards), it is suggested to use TI DIMM100 Controller Boards. If custom Controller Boards are used follow pin functions given in this table: GPIO = general purpose inputs/outputs, PWM = pulse width modulator output pins, CAP = capture input pins, QEP = quadrature encoder input pins, SCI = serial communication interface pins, CAN = controller area network pins, I2C = inter integrated circuit pins, TZ = trip zone pin

Connections – Power Stage (J2)

LARA-100 Motherboard has 40-pin male connector (Molex 0557634070: 2 row, 2 mm pitch, 5 mm row spacing, shrouded header connector) for connection with the same connector type on *PERUN Power Stage*. Through this connector Controller Board provides all command and PWM signals, and receives all protection and measuring signals needed for full-control of *PERUN Power Stage* and its components. All signals are appropriately, safely and precisely conditioned for connected +3.3 V controller systems. User can use originally wired female connector (Molex 0512424000 with Molex 0561349000 contact crimps), provided by PERUN Technologies, for Motherboard and Power Stage connection.

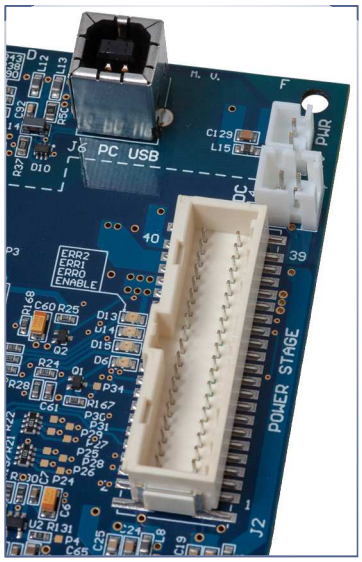


Figure 12: Power stage connector J2

A pin assignment of power stage connector is given in following table:

Table 2: Pin assignment of power stage connector (J2)

Pin	Signal	Description
1	PWM_U	PWM signal for phase-U upper SiC Mosfet gate driver in Power Stage three-phase inverter. It is +5 V active low digital signal.
2	N.C.	Not used.
3	PWM_X	PWM signal for phase-U lower SiC Mosfet gate driver in Power Stage three-phase inverter. It is +5 V active low digital signal.
4	N.C.	Not used.
5	PWM_V	PWM signal for phase-V upper SiC Mosfet gate driver in Power Stage three-phase inverter. It is +5 V active low digital signal.
6	N.C.	Not used.
7	PWM_Y	PWM signal for phase-V lower SiC Mosfet gate driver in Power Stage three-phase inverter. It is +5 V active low digital signal.
8	FDB_VWU	Digital feedback signal providing the state of Power Stage three-phase inverter output voltage between phase-W and phase-U. Not connected.
9	PWM_W	PWM signal for phase-W upper SiC Mosfet gate driver in Power Stage three-phase inverter. It is +5 V active low digital signal.
10	FDB_VUV	Digital feedback signal providing the state of Power Stage three-phase inverter output voltage between phase-U and phase-V. Not connected.
11	PWM_Z	PWM signal for phase-W lower SiC Mosfet gate driver in Power Stage three-phase inverter. It is +5 V active low digital signal.
12	FDB_R	Digital feedback signal providing the state of PERUN Power Stage three-phase diode rectifier phase-R input voltage. It is +5 V active low signal.
13	PWM_EN	PWM enable signal. It is +5 V active low digital signal.
14	FDB_S	Digital feedback signal providing the state of PERUN Power Stage three-phase diode rectifier phase-S input voltage. It is +5 V active low signal.
15	ERR_ACK	Error acknowledgment signal. It is +5 V active low digital signal.

Pin	Signal	Description
16	FDB_T	Digital feedback signal providing the state of PERUN Power Stage three-phase diode rectifier phase-T input voltage. It is +5 V active low signal.
17	CMD_BR	Turn ON/OFF signal for PERUN Power Stage braking chopper circuit. It is +5V active low digital signal.
18	FDB_RST	Digital feedback signal providing the state of PERUN Power Stage three-phase diode rectifier input three-phase voltage. It is +5 V active low signal.
19	CMD_THY	Turn ON/OFF signal for PERUN Power Stage precharge thyristor circuit. It is +5 V active low digital signal.
20	N.C.	Not used.
21	ERR_IALL	Hardware overcurrent protection signal. Overcurrent in any of PERUN Power Stage three-phase inverter output lines will trigger this error. It is +5 V active low digital signal. Overcurrent trigger level is defined by Power Stage hardware (2.5 x nominal current amplitude). Overall overcurrent trigger level can be further configured by software[1)].
22	N.C.	Not used.
23	ERR_VDC	Hardware DC bus overvoltage protection signal. It is +5 V active low digital signal. Overvoltage trigger level is defined by PERUN Power Stage hardware (790 V). Overall DC overvoltage trigger level can be further configured by software[2)].
24	FDB_VDC	Analog feedback signal providing measured value of DC bus voltage. This pin accepts analog 0-10 V voltage signal. Gain of DC bus voltage measurement circuit can be further configured by software[3)].
25	ERR_TEMP	Over-temperature protection signal. It is +5 V active low digital signal.
26	FDB_IW	Analog feedback signal providing measured value of PERUN Power Stage three-phase inverter phase-W output current. This pin accepts analog -10 V – 10 V voltage signal. Gain of current measurement circuit can be further configured by software[4)].
27	FDB_TEMP	Analog feedback signal providing measured value of PERUN Power Stage averaged semiconductor temperature. This pin accepts analog 0-10 V voltage signal. Gain of measurement circuit is fixed.

Pin	Signal	Description
28	FDB_IV	Analog feedback signal providing measured value of PERUN Power Stage three-phase inverter phase-V output current. This pin accepts analog -10 V – 10 V voltage signal. Gain of current measurement circuit can be further configured by software[4)].
29	CMD_VENT	Turn ON/OFF command signal for Power Stage heatsink ventilators. It is +5 V active low digital signal.
30	FDB_IU	Analog feedback signal providing measured value of PERUN Power Stage three-phase inverter phase-U output current. This pin accepts analog -10 V – 10 V voltage signal. Gain of current measurement circuit can be configured by software[4)].
31	GND	Electronics ground reference.
32	GND	Electronics ground reference.
33	GND	Electronics ground reference.
34	GND	Electronics ground reference.
35	+5V	+5 V power supply for digital circuits. Needed +3.3 V voltage for digital circuits is generated with on-board voltage regulator. All power rails are filtered on Motherboard.
36	+5V	+5 V power supply for digital circuits. Needed +3.3 V voltage for digital circuits is generated with on-board voltage regulator. All power rails are filtered on Motherboard.
37	+5V	+5 V power supply for digital circuits. Needed +3.3 V voltage for digital circuits is generated with on-board voltage regulator. All power rails are filtered on Motherboard.
38	+5V	+5 V power supply for digital circuits. Needed +3.3 V voltage for digital circuits is generated with on-board voltage regulator. All power rails are filtered on Motherboard.
39	+15V	+15 V power supply for analog circuits. Needed +5 V, -5 V, +3.3 V, +2.5 V and -2.5 V voltages for analog circuits are generated from this voltage with on-board voltage regulators. All power rails are filtered on Motherboard.
40	-15V	-15 V power supply for analog circuits. All power rails are filtered on Motherboard.

Signals functions are clearly designated in following principal schematic which includes Power Stage topology.

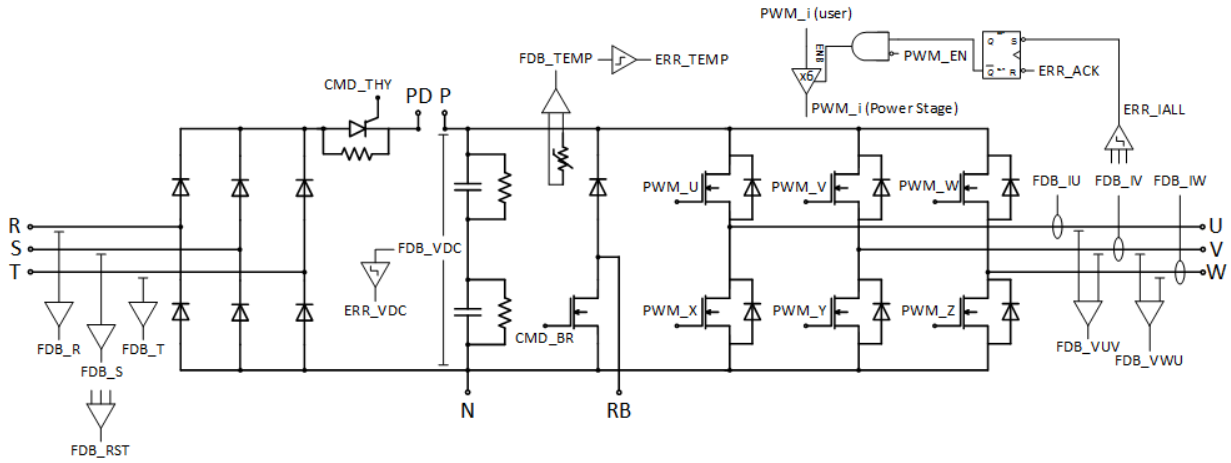


Figure 13: Principle schematic of LARA-100 power stage

Connections – GPIO Board connector (J3)

LARA-100 Motherboard has 60-pin male connector (Samtec TW-30-06-F-D-291-SM-000: 2 row, 2 mm pitch, flexible board stacker) for connection with PERUN's GPIO Boards. Through this connector and GPIO Board user can expand functionality of the whole LARA-100 system through general purpose digital and analog inputs and outputs. Pinout interface between TI DIMM100 Controller Boards and GPIO Boards is carefully designed not to occupy pins required for PERUN Power Stage control. GPIO Boards usually features power PCB relay modules, open-collector or fiber-optical digital outputs, optocoupler or fiber-optical digital inputs, bipolar -10V/+10V and unipolar 0/+10V voltage analog inputs, 0/20mA and 4/20mA current analog inputs, SPI or I2C digital-to-analog converters for voltage and current analog outputs, and isolation circuits between user and controller sides. Moreover, PWM and measurement feedback signals are available on GPIO connector allowing connection of two LARA-100 converters in back-to-back configuration through specialized GPIO Board.

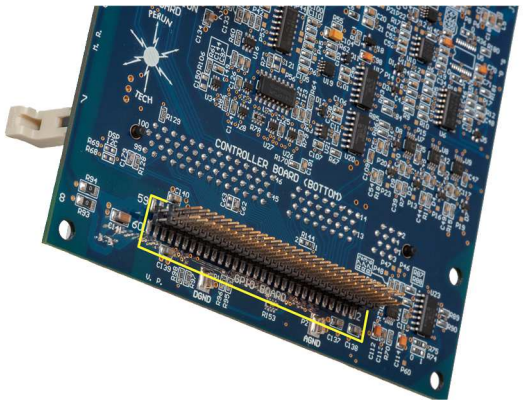


Figure 14 LARA 100 GPIO board connector (J3)

Pin assignments of GPIO Board connector related to the Controller Board (TI DIMM100 controlCards) is given in following table:

Table 3: Pin assignment of GPIO board connector (J1)

Pin	Signal	Description
1	GND	Ground reference for GPIO Board power supply (+3.3V, +5V, -15V, and +15V).
2	-15V	-15 V power supply for analog circuits on GPIO Board.
3	GND	Ground reference for GPIO Board power supply (+3.3V, +5V, -15V, and +15V).
4	+15V	+15 V power supply for analog circuits on GPIO Board.
5	DSP_IU/ADCIN-A0	Measured and conditioned signal (0-3V) of PERUN Power Stage three-phase inverter phase-U output current which is also directly connected to the Controller Board analog input (ADCIN-A0 at TI controlCard).
6	ADCIN-B0	Pin directly connected to Controller Board analog input ADCIN-B0.
7	DSP_IU/ADCIN-A1	Measured and conditioned signal (0-3V) of PERUN Power Stage three-phase inverter phase-V output current which is also directly connected to the Controller Board analog input ADCIN-A1.
8	ADCIN-B1	Pin directly connected to Controller Board analog input ADCIN-B1.
9	DSP_IW/ADCIN-A2	Measured and conditioned signal (0-3V) of PERUN Power Stage three-phase inverter phase-W output current which is also directly connected to the Controller Board analog input ADCIN-A2.
10	ADCIN-B2	Pin directly connected to Controller Board analog input ADCIN-B2.
11	ADCIN-B4	Pin directly connected to Controller Board analog input ADCIN-B4.
12	ADCIN-B5	Pin directly connected to Controller Board analog input ADCIN-B5.
13	ADCIN-A6	Pin directly connected to Controller Board analog input ADCIN-A6.
14	ADCIN-B6	Pin directly connected to Controller Board analog input ADCIN-B6.
15	GPIO-61	Pin directly connected to Controller Board general purpose input/output GPIO-61.
16	DSP_VDC/ADCIN-A3	By default, this pin features measured and conditioned

Pin	Signal	Description
		signal (0-3V) of PERUN Power Stage DC bus voltage which is also directly connected to the Controller Board analog input ADCIN-A3.
17	GPIO-63/SCITX-C	Pin directly connected to Controller Board general purpose input/output GPIO-63. On some GPIO Boards this pin function as serial communication interface transmit (TX) pin.
18	GPIO-60	Pin directly connected to Controller Board general purpose input/output GPIO-60.
19	DSP_GX/GPIO-01/EPWM-1B	This pin features controller PWM command signal DSP_GX for switching PERUN Power Stage phase-U lower SiC Mosfet and which is directly connected to the Controller Board PWM output GPIO-01/EPWM-1B.
20	GPIO-62/SCIRX-C	Pin directly connected to Controller Board general purpose input/output GPIO-62. On some GPIO Boards this pin function as serial communication interface receive (RX) pin.
21	DSP_GY/GPIO-03/EPWM-2B	This pin features controller PWM command signal DSP_GY for switching PERUN Power Stage phase-V lower SiC Mosfet and which is directly connected to the Controller Board PWM output GPIO-03/EPWM-2B.
22	DSP_GU/GPIO-00/EPWM-1A	This pin features controller PWM command signal DSP_GU for switching PERUN Power Stage phase-U upper SiC Mosfet and which is directly connected to the Controller Board PWM output GPIO-00/EPWM-1A.
23	DSP_GZ/GPIO-05/EPWM-3B	This pin features controller PWM command signal DSP_GZ for switching PERUN Power Stage phase-W lower SiC Mosfet and which is directly connected to the Controller Board PWM output GPIO-05/EPWM-3B.
24	DSP_GV/GPIO-02/EPWM-2A	This pin features controller PWM command signal DSP_GV for switching PERUN Power Stage phase-V upper SiC Mosfet and which is directly connected to the Controller Board PWM output GPIO-02/EPWM-2A.
25	GPIO-06/EPWM-4A	Pin directly connected to Controller Board general purpose input/output GPIO-06. On some GPIO Boards this pin function as PWM output (e.g. for controlling another LARA-100 converter).
26	DSP_GW/GPIO-04/EPWM-3A	This pin features controller PWM command signal DSP_GW for switching PERUN Power Stage phase-W upper SiC Mosfet and which is directly connected to the Controller Board PWM output GPIO-04/EPWM-3A.

Pin	Signal	Description
27	GPIO-09/EPWM-5B	Pin directly connected to Controller Board general purpose input/output GPIO-09. On some GPIO Boards this pin function as PWM output (e.g. for controlling another LARA-100 converter).
28	GPIO-07/EPWM-4B	Pin directly connected to Controller Board general purpose input/output GPIO-07. On some GPIO Boards this pin function as PWM output (e.g. for controlling another LARA-100 converter).
29	GPIO-11/EPWM-6B	Pin directly connected to Controller Board general purpose input/output GPIO-11. On some GPIO Boards this pin function as PWM output (e.g. for controlling another LARA-100 converter).
30	GPIO-08/EPWM-5A	Pin directly connected to Controller Board general purpose input/output GPIO-08. On some GPIO Boards this pin function as PWM output (e.g. for controlling another LARA-100 converter).
31	DSP_VUV/GPIO-48	This pin features conditioned digital feedback signal (0-3.3V) providing the state of Power Stage three-phase inverter output voltage between phases U and V, and which is directly connected to the Controller Board digital input GPIO-48.
32	GPIO-10/EPWM-6A	Pin directly connected to Controller Board general purpose input/output GPIO-10. On some GPIO Boards this pin function as PWM output (e.g. for controlling another LARA-100 converter).
33	GPIO-25/ECAP-2/EQEPB-2	Pin directly connected to Controller Board general purpose input/output GPIO-25. On some GPIO Boards this pin function as capture (CAP) or quadrature encoder (QEP) input.
34	GPIO-14/TZ-3/SCITX-B	Pin directly connected to Controller Board general purpose input/output GPIO-14. On some GPIO Boards this pin function as PWM disable/error trigger (TZ) input or as serial communication interface transmit (TX) pin.
35	GPIO-15/TZ-4/SCIRX-B	Pin directly connected to Controller Board general purpose input/output GPIO-15. On some GPIO Boards this pin function as PWM disable/error trigger (TZ) input or as serial communication interface receive (RX) pin.
36	GPIO-24/ECAP-1/EQEPA-2	Pin directly connected to Controller Board general purpose input/output GPIO-24. On some GPIO Boards this pin function as capture (CAP) or quadrature encoder (QEP)

Pin	Signal	Description
		input.
37	GPIO-27/ECAP-4/EQEPS-2	Pin directly connected to Controller Board general purpose input/output GPIO-24. On some GPIO Boards this pin function as capture (CAP) or quadrature encoder (QEP) input.
38	GPIO-26/ECAP-3/EQEPI-2	Pin directly connected to Controller Board general purpose input/output GPIO-26. On some GPIO Boards this pin function as capture (CAP) or quadrature encoder (QEP) input.
39	GPIO-19/SPISTE-A/SCIRX-B	Pin directly connected to Controller Board general purpose input/output GPIO-19. On some GPIO Boards this pin function as serial peripheral interface (SPI) bus select (STE) pin or serial communication interface receive (RX) pin.
40	GPIO-17/SPISOMI-A/CANRX-B	Pin directly connected to Controller Board general purpose input/output GPIO-17. On some GPIO Boards this pin function as SPI bus SOMI/MISO pin or CAN bus receive (RX) pin.
41	GPIO-16/SPISIMO-A/CANTX-B	Pin directly connected to Controller Board general purpose input/output GPIO-16. On some GPIO Boards this pin function as SPI bus SIMO/MOSI pin or CAN bus transmit (TX) pin.
42	GPIO-18/SPICLK-A/SCITX-B	Pin directly connected to Controller Board general purpose input/output GPIO-18. On some GPIO Boards this pin function as SPI bus clock (CLK) pin or serial communication interface transmit (TX) pin.
43	GPIO-33/I2CSCL	Pin directly connected to Controller Board general purpose input/output GPIO-33. On some GPIO Boards this pin function as I2C bus clock (CLK) pin.
44	GPIO-31/CANTX-A	Pin directly connected to Controller Board general purpose input/output GPIO-31. On some GPIO Boards this pin function as CAN bus transmit (TX) pin.
45	GPIO-30/CANRX-A	Pin directly connected to Controller Board general purpose input/output GPIO-30. On some GPIO Boards this pin function as CAN bus receive (RX) pin.
46	ERR_GPIO	Protection digital input dedicated for direct setting LARA-100 system in error state through GPIO Board (e.g. with connected panic button). Low 0V signal on this pin will immediately activate error signal and disable PWM signals on Motherboard.

Pin	Signal	Description
47	GPIO-32/I2CSDA	Pin directly connected to Controller Board general purpose input/output GPIO-32. On some GPIO Boards this pin function as I2C bus data (SDA) pin.
48	ERR_RST_GPIO	Digital input dedicated for acknowledging and clearing LARA-100 system error state through GPIO Board (e.g. with connected switch button). Low 0V signal on this pin will reset error signal and enable PWM signals on Motherboard.
49	SCL	Pin reserved for communication link with PERUN PowerDesk software through Motherboard USB connection.
50	SDA	Pin reserved for communication link with PERUN PowerDesk software through Motherboard USB connection.
51	GND	Ground reference for GPIO Board power supply (+3.3V, +5V, -15V, and +15V).
52	ERR	This pin features Motherboard error signal. It is used for monitoring and signaling LARA-100 system error state. This output is active low (0V).
53	GND	Ground reference for GPIO Board power supply (+3.3V, +5V, -15V, and +15V).
54	+5V	+5V power supply for digital circuits on GPIO Board.
55	+3.3V	+3.3V power supply for digital circuits on GPIO Board.
56	+5V	+5V power supply for digital circuits on GPIO Board.
57	N.C.	Not connected.
58	N.C.	Not connected.
59	GND_ISO	Isolated ground reference for +24V_ISO power supply (user side ground). GND_ISO is isolated from GND.
60	+24V_ISO	Isolated +24 V power supply. By default, this power supply is available for GPIO Board from PERUN Power Stage through Motherboard connector (J11).

GPIO Board connector (J3) pinout definition is shown in the figure below.

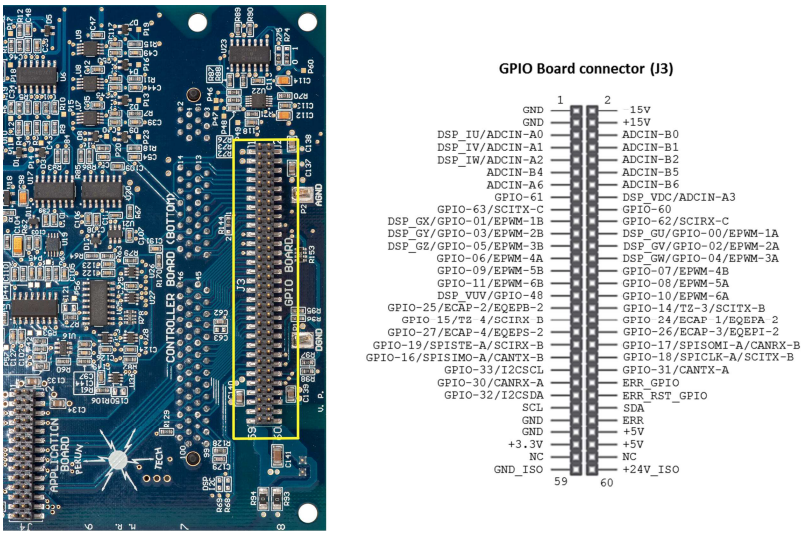


Figure 15: GPIO Board connector - pinout definition

Connections – Application Board connector (J4)

LARA-100 Motherboard has 28-pin male connector (Samtec TW-14-07-F-D-350-SM-000: 2 row, 2 mm pitch, flexible board stacker) for connection with PERUN's Application Boards. Through this connector and Application Board user can adapt his LARA-100 system to specific power electronics application. Either it is a motor drive or PV boost converter or grid-connected converter user can transform his LARA-100 system simply by adding or replacing the Application Board. Pinout interface between TI DIMM100 Controller Boards and Application Boards is carefully designed to cover wide range of power electronics applications which include use of specific controller peripherals such as capture inputs (CAP), quadrature encoder inputs (QEP), analog inputs (ADCIN) and communication buses (SPI/I2C).

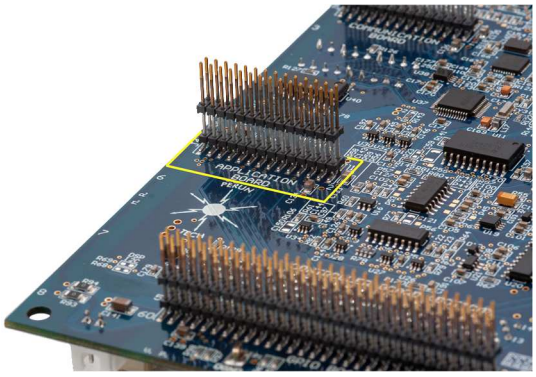


Figure 16: LARA-100 Motherboard's Application Board connector

Through Application Boards all these peripherals are adapted for direct connection of user external devices like quadrature or absolute encoders, resolvers, grid lines and PV panels/strings (for voltage and additional current measurement) and others. All signals are galvanically isolated between the user and controller, assuring safe interfacing with eliminated noise influence.

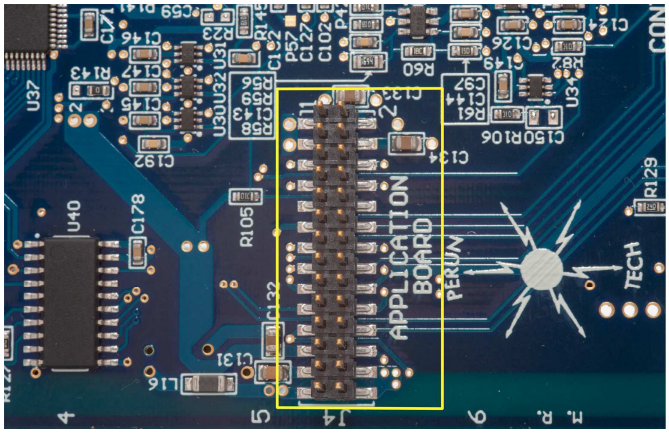
Pin assignments of Application Board connector related to the Controller Board (TI DIMM100 controlCards) is given in following table:

Table 4: Pin assignment of application board connector (J4)

Pin	Signal	Description
1	GND	Ground reference for Application Board power supply (+3.3V, +5V, -15V, and +15V).
2	-15V	-15 V power supply for analog circuits on Application Board.
3	GND	Ground reference for Application Board power supply (+3.3V, +5V, -15V, and +15V).
4	+15V	+15 V power supply for analog circuits on Application Board.
5	ADCIN-B3	Pin directly connected to Controller Board analog input ADCIN-B3. On analog input pins, Application Board mainly provides measured signals like grid or PV voltages, resolver position/speed signals, tacho-generator speed signal, additional current measurement etc.
6	ADCIN-B2	Pin directly connected to Controller Board analog input ADCIN-B2.
7	ADCIN-B1	Pin directly connected to Controller Board analog input ADCIN-B1.
8	ADCIN-B0	Pin directly connected to Controller Board general purpose input/output GPIO-25. On some Application Boards this pin functions as capture input (CAP) or as quadrature encoder input (QEPB), mainly for connection with motor speed sensors like encoders.
9	GPIO-25/ECAP-2/EQEPB-2	Protection digital input dedicated for direct setting LARA-100 system in error state through Application Board (e.g. motor overspeed or grid/PV overvoltage error). Low signal (0 V) on this pin will immediately activate Motherboard error signal and disable all PWM signals.
10	ERR_APP	Protection digital input dedicated for direct setting LARA-100 system in error state through Application Board (e.g. motor overspeed or grid/PV overvoltage error). Low signal (0 V) on this pin will immediately activate Motherboard error signal and disable all PWM signals.
11	GPIO-17/SPISOMI-A	Pin directly connected to Controller Board general purpose input/output GPIO-17. On some Application Boards this pin function as SPI bus SOMI/MISO pin for communication with specific on-board circuits.
12	GPIO-24/ECAP-	Pin directly connected to Controller Board general purpose

Pin	Signal	Description
	1/EQEPA-2	input/output GPIO-24. On some Application Boards this pin functions as capture input (CAP) or as quadrature encoder input (QEPA), mainly for connection with motor speed sensors like encoders.
13	GPIO-19/SPISTE-A	Pin directly connected to Controller Board general purpose input/output GPIO-19. On some Application Boards this pin function as SPI bus select pin for communication with specific on-board circuits.
14	GPIO-16/SPISIMO-A	Pin directly connected to Controller Board general purpose input/output GPIO-16. On some Application Boards this pin function as SPI bus SIMO/MOSI pin for communication with specific on-board circuits.
15	GPIO-21/EQEPB-1	Pin directly connected to Controller Board general purpose input/output GPIO-21. On some Application Boards this pin function as quadrature encoder input (QEPB), mainly for connection with motor speed sensors like encoders.
16	GPIO-18/SPICLK-A	Pin directly connected to Controller Board general purpose input/output GPIO-18. On some Application Boards this pin function as SPI bus CLK pin for communication with specific on-board circuits.
17	GPIO-23/EQEPI-1	Pin directly connected to Controller Board general purpose input/output GPIO-23. On some Application Boards this pin function as encoder index input (QEPI), mainly for connection with motor speed sensors like encoders.
18	GPIO-20/EQEPA-1	Pin directly connected to Controller Board general purpose input/output GPIO-20. On some Application Boards this pin function as quadrature encoder input (QEPA), mainly for connection with motor speed sensors like encoders.
19	GPIO-33/I2CSCL	Pin directly connected to Controller Board general purpose input/output GPIO-33. On some Application Boards this pin function as I2C bus SCL clock pin for communication with specific on-board circuits.
20	GPIO-22/EQEPS-1	Pin directly connected to Controller Board general purpose input/output GPIO-22. On some Application Boards this pin function as encoder strobe input (QEPS), mainly for connection with motor speed sensors like encoders.
21	SDA	Pin reserved for communication link with PERUN PowerDesk software through Motherboard USB connection.
22	GPIO-32/I2CSDA	Pin directly connected to Controller Board general purpose

Pin	Signal	Description
		input/output GPIO-32. On some Application Boards this pin function as I2C bus SDA clock pin for communication with specific on-board circuits.
23	+3.3V	+3.3V power supply for digital circuits on Application Board.
24	SCL	Pin reserved for communication link with PERUN PowerDesk software through Motherboard USB connection.
25	+5V	+5V power supply for digital circuits on Application Board.
26	GND	Ground reference for Application Board power supply (+3.3V, +5V, -15V, and +15V).
27	+5V	+5V power supply for digital circuits on Application Board.
28	GND	Ground reference for Application Board power supply (+3.3V, +5V, -15V, and +15V).



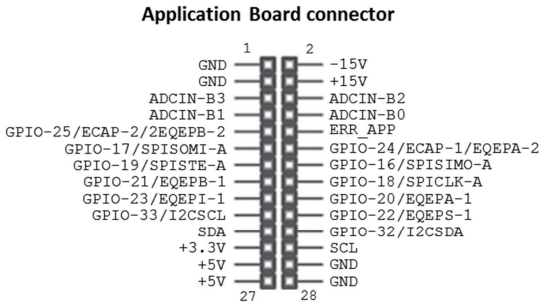


Figure 17: Application Board connector - pinout definition

Communication Board connector (J5)

LARA-100 Motherboard has 28-pin male connector (Samtec TW-14-07-F-D-350-SM-000: 2 row, 2 mm pitch, flexible board stacker) for connection with PERUN's Communication Boards. Through this connector and Communication Board user can connect its Controller Board with external devices

through various communication buses such as Ethernet, CAN, RS-485, RS-232, USB/UART, or JTAG. Two or more LARA-100 systems, each with its own controller, can be connected through appropriate communication link for building more complex converter systems. For example, for building PV inverter consisting of boost converter and grid-connected inverter user could connect two LARA-100 systems through CAN bus for communication and exchanging command, measurement, state and other data between their controllers (see EPFL user story). Moreover, using one of the standard communication buses available through Communication Boards user can connect several independent LARA-100 systems (programmed for specific task) to the supervisory controller for building larger systems like micro and smart grids. All signals are galvanically isolated between the user and controller sides, assuring safe interfacing with eliminated noise influence.

Pin assignments of Communication Board connector related to the Controller Board (TI DIMM100 controlCards) is given in following table.

Table 5: Pin assignment of analog outputs connector

Pin	Signal	Description
1	+3.3V	+3.3 V power supply for digital circuits on Application Board.
2	+5 V	+5 V power supply for digital circuits on Application Board.
3	GND	Ground reference for Communication Board power supply (+3.3V and +5V).
4	+5 V	+5 V power supply for digital circuits on Application Board.
5	GPIO-17/SPISOMI-A/CANRX-B	Pin directly connected to Controller Board general purpose input/output GPIO-17. Depending on Application Board this pin can function as SPI bus SOMI/MISO pin or CAN bus receive (RX) pin.
6	+3.3V	+3.3 V power supply for digital circuits on Application Board.
7	GPIO-19/SPISTE-A/SCIRX-B	Pin directly connected to Controller Board general purpose input/output GPIO-19. Depending on Application Board this pin can function as SPI bus select pin or serial communication interface (SCI) receive (RX) pin.
8	GPIO-16/SPISIMO-A/CANTX-B	Pin directly connected to Controller Board general purpose input/output GPIO-16. Depending on Application Board this pin can function as SPI bus SIMO/MOSI pin or CAN bus transmit (TX) pin.
9	GPIO-63/SCITX-C	Pin directly connected to Controller Board general purpose input/output GPIO-63. On some Communication Boards this pin function as serial communication interface (SCI)

Pin	Signal	Description
		transmit (TX) pin.
10	GPIO-18/SPICLK-A/SCITX-B	Pin directly connected to Controller Board general purpose input/output GPIO-18. Depending on Application Board this pin can function as SPI bus CLK clock pin or serial communication interface (SCI) transmit (TX) pin.
11	TXD_DSP	Serial communication interface (SCI) transmit (TX) pin reserved for communication between Controller Board and PERUN PowerDesk software.
12	GPIO-62/SCIRX-C	Pin directly connected to Controller Board general purpose input/output GPIO-62. On some Communication Boards this pin function as serial communication interface (SCI) receive (RX) pin.
13	GPIO-31/CANTX-A	Pin directly connected to Controller Board general purpose input/output GPIO-31. On some Communication Boards this pin function as CAN bus transmit (TX) pin.
14	RXD_DSP	Serial communication interface (SCI) receive(RX) pin reserved for communication between Controller Board and PERUN PowerDesk software.
15	GPIO-33/I2SCL	Pin directly connected to Controller Board general purpose input/output GPIO-33. On some Communication Boards this pin function as I2C bus SCL clock pin.
16	GPIO-30/CANRX-A	Pin directly connected to Controller Board general purpose input/output GPIO-30. On some Communication Boards this pin function as CAN bus receive (RX) pin.
17	JTAG_RTCK	JTAG communication bus pin for return clock (RTCK) signal from Motherboard. Reserved for proper JTAG communication.
18	GPIO-32/I2CSDA	Pin directly connected to Controller Board general purpose input/output GPIO-32. On some Communication Boards this pin function as I2C bus SDA data pin.
19	GND	Ground reference for Communication Board power supply (+3.3V and +5V).
20	JTAG_TCK	Pin connected to Controller Board JTAG interface TCK pin.
21	JTAG_TDI	Pin connected to Controller Board JTAG interface TDI pin.
22	JTAG_TMS	Pin connected to Controller Board JTAG interface TMS pin.
23	JTAG_TRSTn	Pin connected to Controller Board JTAG interface TRSTn pin.

Pin	Signal	Description
24	JTAG_TDO	Pin connected to Controller Board JTAG interface TDO pin.
25	JTAG_EMU0	Pin connected to Controller Board JTAG interface EMU0 pin.
26	JTAG_EMU1	Pin connected to Controller Board JTAG interface EMU1 pin.
27	SDA	Pin reserved for communication link with PERUN PowerDesk software through Motherboard USB connection.
28	SCL	Pin reserved for communication link with PERUN PowerDesk software through Motherboard USB connection.

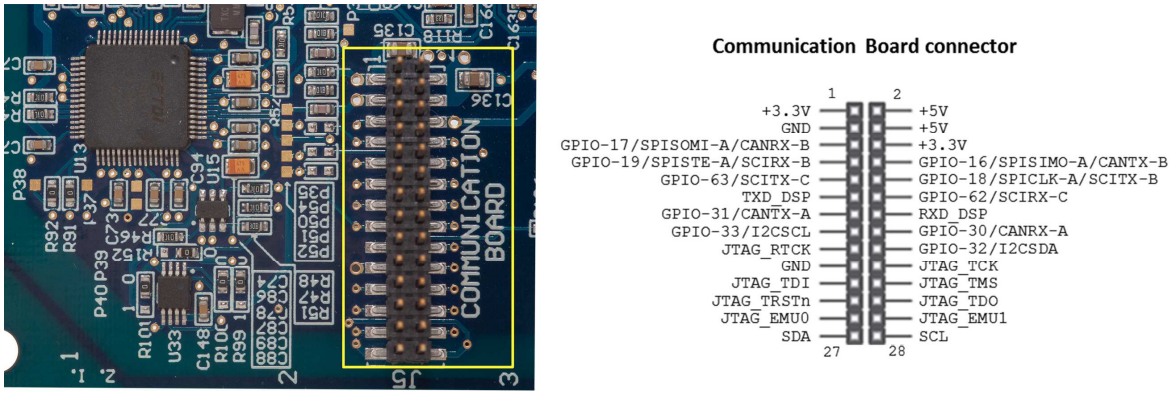


Figure 18: Communication board connector - pinout definition

Connections – USB connector (J6) and +24V Isolated Power Supply connector (J10)

USB connector (J6) – LARA-100 Motherboard has standard USB-B 4-pin receptacle connector (TE Connectivity part number: 5787834-1) for connection with PERUN PowerDesk software. On-board USB to UART/I2C/JTAG bridge circuit allows communication between PERUN PowerDesk software and LARA-100 hardware components: Motherboard, GPIO, Application and Communication Boards, including plugged-in Controller Board. In this manner, through PERUN PowerDesk user is capable to configure and monitor its LARA-100 hardware components, and to program, debug, control and monitor connected Controller Board.

+24V Isolated Power Supply connector (J10) – LARA-100 Motherboard has 2-pin male connector (JST part number B2B-XH-A(LF)(SN); 2.5 mm pitch, shrouded header connector) for connection with the same connector type on Power Stage which supplies +24 V power isolated from +5 V and ±15 V. This isolated power supply is used on GPIO Board connector for powering circuits on user side of GPIO Boards. Use originally wired female connector (JST XHP-2 with JST SXH-001T-P0.6 contact crimps), provided by PERUN Technologies, for Motherboard and PERUN Power Stage connection.

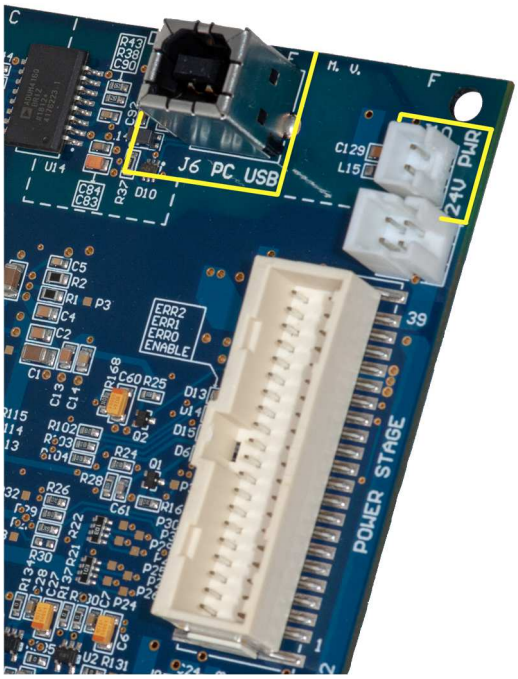


Figure 19: LARA 100 USB connector and +24V Isolated Power Supply connector

3 TECHNICAL DATA

General technical data are given in the following table:

Table 6: Technical data – general overview

Feature		Value
Electrical Rating	Nominal operating voltage for digital circuits +5V (J2-35,36,37,38)	+5 VDC (+4.8…+5.2 VDC)
	Nominal operating voltage for analog circuits ±15V (J2-39, 40)	J2-39 = +15 VDC (+14…+16 VDC) J2-40 = -15 VDC (-14…-16 VDC)
	Nominal operating voltage for isolated power +24V_ISO (J10-1)	+24 VDC (+22…+25 VDC) isolated from +5V and ±15V power rails
	Nominal operating voltage for Controller Board +5V (J1-54,64,74,84,92)	+5 VDC
	Nominal operating voltage for controller on Controller Board (internal on Controller Board)	+3.3 VDC (Motherboard is designed for +3.3 V controllers; Controller Board must have built-in +5V to +3.3 power regulator)
	Nominal operating voltages on GPIO interface J3	J3-53 = +3.3 VDC (for digital circuits) J3-54,56 = +5 VDC (for digital circuits) J3-2 = -15 VDC (for analog circuits) J3-4 = +15 VDC (for analog circuits) J3-60 = +24V VDC (for isolated/user side circuits)
	Nominal operating voltages on APP interface J4	J4-23 = +3.3 VDC (for digital circuits) J4-25,27 = +5 VDC (for digital circuits) J4-2 = -15 VDC (for analog circuits) J4-4 = +15 VDC (for analog circuits)
	Nominal operating voltages on COMM interface J5	J5-1,6 = +3.3 VDC J5-2,4 = +5 VDC
	Input current (J2 interface)	0.8 – 2 A @+5V (depending on connected interfaces) 0.2 – 0.5 A @±15 V (depending on connected

Feature		Value
		interfaces)
Inputs & Outputs	PWM outputs	@J1 Controller interface: +3.3 VDC @J2 Power Stage interface: +5 VDC @J3 GPIO interface: +3.3 VDC
	Protection/error inputs and outputs	@J1 Controller interface: +3.3 VDC @J2 Power Stage interface: +5 VDC @J3 GPIO interface: +3.3 VDC @J4 APP interface: +3.3 VDC
	Digital inputs and outputs	@J1 Controller interface: +3.3 VDC @J2 Power Stage interface: +5 VDC @J3 GPIO interface: +3.3 VDC @J4 APP interface: +3.3 VDC @J5 COMM interface: +3.3 VDC
	Analog/feedback inputs	@J1 Controller interface: 0…+3 V @J2 Power Stage interface: -10…+10 V @J3 GPIO interface: 0…3 V all referenced to GND
Status Indicators	Enable PWM operation	Green LED D6 (EN)
	Error	Red LEDs D13, D14, D15 (ERR2, ERR1, ERR0)
Physical	Dimensions (L x W x H)	165.0 x 114.4 x 40.0 mm
	Weight	approx. 300 g

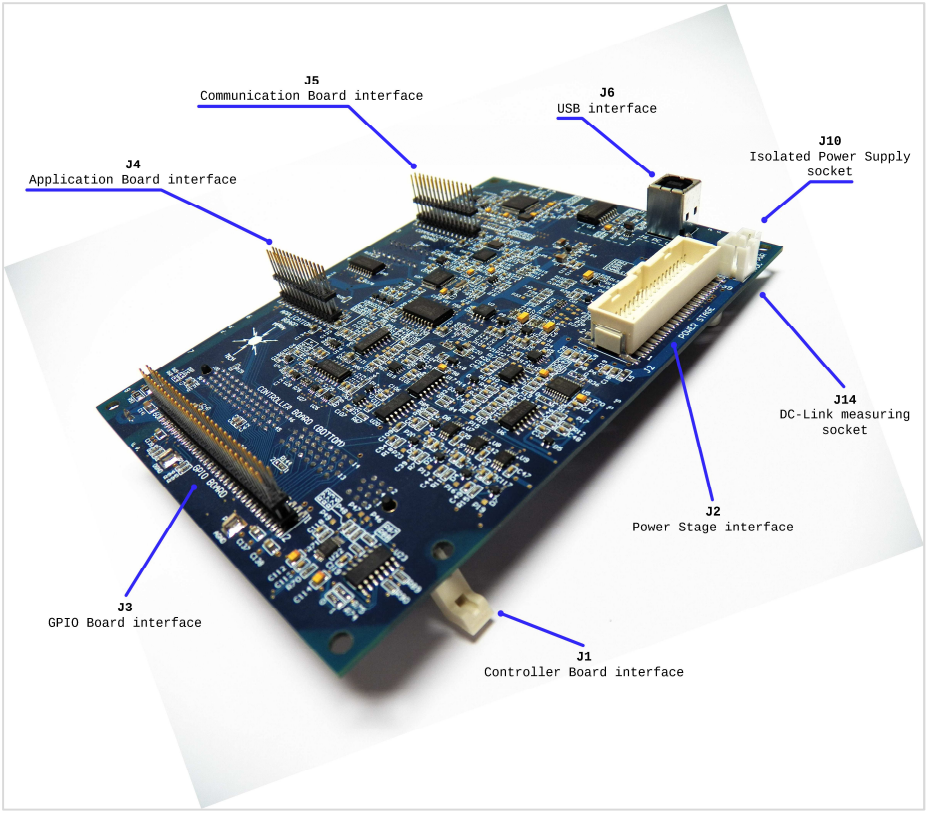


Figure 20: Interface overview of LARA-100 Motherboard

3.1 PWM OUTPUTS CIRCUIT

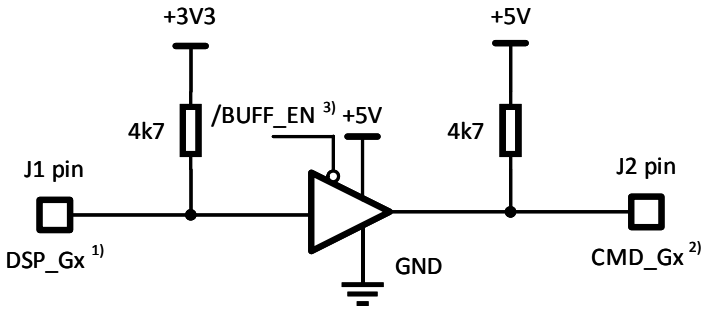


Figure 21: PWM outputs circuit (shown for one PWM output) – functional overview

1) DSP_Gx are controller PWM outputs at J1 Controller Board interface (x = U, X, V, Y, W, Z).

2) CMD_Gx are PWM outputs at J2 Power Stage interface (x = U, X, V, Y, W, Z).

[3] /BUFF_EN is PWM buffer enable signal. Its state is determined by controller PWM enable signal (PWM_EN/GPIO-49), global error signal (ERR), and global error reset signal (ERR_RST). For more details, see section “PWM enable circuit”.

Table 7: PWM outputs – technical data

Data	Value
Voltage level	0/+3.3 VDC (@J1 interface) 0/+5 VDC (@J2 interface)
Active level (logic 1)	0 V; typically < 1.0 V
Inactive level (logic 0)	+3.3 V (@J1 interface); typically > 2.4 V +5 V (@J2 interface); typically > 3.8 V
Pull-ups	4.7 kΩ (@J1 interface; assure inactive logic level also if there is no plugged-in Controller Board) 4.7 kΩ (@J2 interface)

3.2 PROTECTION LOGIC – ERROR SIGNAL GENERATION CIRCUIT

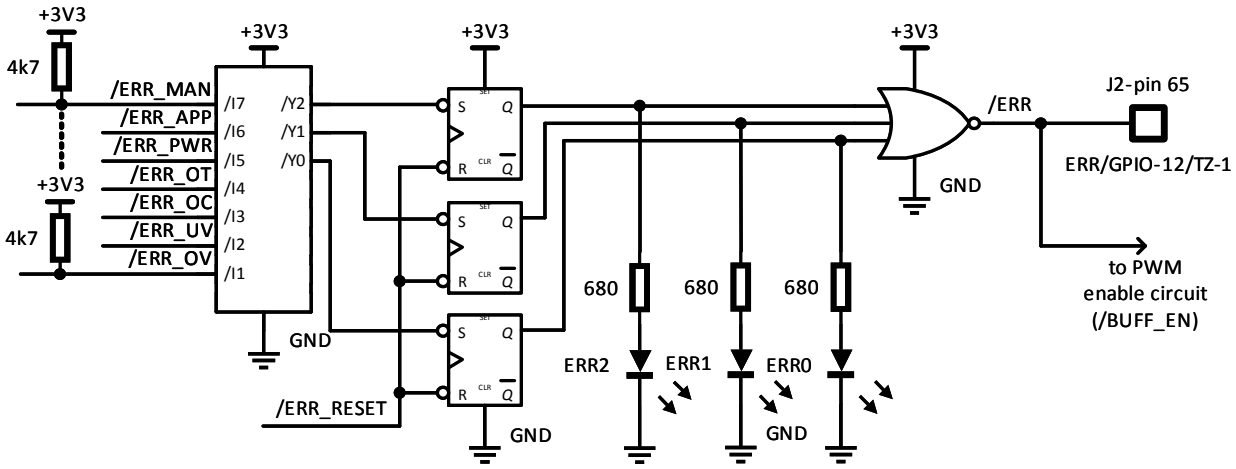


Figure 22: Protection logic – functional overview

Table 8: Protection logic – technical data

Data	Signal / Value
Global error (output) signal	/ERR
Active voltage level for error output signal (/ERR)	0 V
Inactive voltage level for error output signal (/ERR)	+3.3 V
Application Board error signal	/ERR_APP
Power Supply error signal	/ERR_PWR
Overtemperature error signal	/ERR_OT
Overcurrent error signal	/ERR_OC
DC-link undervoltage error signal	/ERR_UV
DC-link overvoltage error signal	/ERR_OV
Active voltage level for error input signals (/ERR_MAN, /ERR_APP, /ERR_PWR, /ERR_OT, /ERR)	0 V; typically < 1.0 V
Inactive voltage level for error input signals	+3.3 V; typically > 2.4 V
Pull-ups at error inputs	4.7 kΩ

The different statuses that arise during the LARA-100 system operation are indicated by means of the LEDs on the Motherboard.

- If an error occurs, PWM pulses (SiC Mosfets gate drive signals) are inhibited and the cause is indicated accordingly via the LEDs. Red error LEDs (ERR2, ERR1, and ERR0) indicates error cause, and switched off green enable LED (EN) indicates that PWM pulses are inhibited.

- Once the error has been successfully acknowledged, all the red error LEDs (ERR2, ERR1, ERR0) are switched off. That means converter is ready for operation, but still user have to enable PWM pulses (green enable LED indicates that PWM pulses are disabled/enabled).

- After Motherboard power-up, all the red error LEDs are switched on indicating manual error state. In other words, during boot-up procedure, system is forced to the error state (source/cause = manual) to disable PWM pulses and to put Power Stage in safe state. Error has to be acknowledged, in order to enable PWM pulses and Power Stage operation after boot up is terminated.

TABLE 8: ERROR STATES AND BEHAVIOR OF THE STATUS LEDS

LED				Status	Signal / Value
EN	ERR2	ERR1	ERR0		
1	0	0	0	Enabled	PWM command signals are enabled and system is ready for operation
0	1	1	1	Manual error	Error occurred due to one of the following manual causes: • Controller error trigger signal ERR_DSP/GPIO-13 • PERUN PowerDesk software error trigger signal • GPIO Board external input error signal
0	1	1	0	Application error	Error occurred due to the Application Board error triggering signal (e.g. grid line overvoltage in the case of APP-UI application board)
0	1	0	1	Power Supply error	Error occurred due to the incorrect +5 V power supply line. Voltage level is either below +4.7 V or above +5.3 V
0	1	0	0	Over-temperature error	Error occurred due to the Power Stage heatsink over-temperature. Heatsink temperature is higher than 95 ^{0}C.
0	0	1	1	Overcurrent error	Error occurred due to the Power Stage inverter's output currents above limits. Current limits are set by: • Power Stage original current rating (2.5 x amplitude of nominal current) • Motherboard current limit settings (by default equal to 2.5 x amplitude of Power Stage nominal current, but can be specified during purchasing process)
0	0	1	0	Undervoltage error	Error occurred due to the Power Stage DC-link voltage below limit value. By default, lower limit for DC-link voltage is set to 300 V, but it can be specified during purchasing process
0	0	0	1	Overvoltage error	Error occurred due to the Power Stage DC-link voltage above limit value. Upper

LED				Status	Signal / Value
EN	ERR2	ERR1	ERR0		
					limit for DC-link voltage is determined by: • Power Stage original setting 790 V • Motherboard DC-link voltage limit settings (by default equal to original setting 790 V, but can be specified during purchasing process)
0	0	0	0	Ready	System is ready for operation, but PWM pulses are still inhibited

Error code is available as analog value at Controller Board interface J1-pin 42 (ERR_CODE/ADCIN-A7). Binary error code (ERR2, ERR1, ERR0) is converted to analog voltage value from 0 to 3 V, according to following rules:

- (ERR2, ERR1, ERR0) = (0, 0, 0) = No error = 0 V ± 0.075 V
- (ERR2, ERR1, ERR0) = (0, 0, 1) = DC-link overvoltage = 0.375 V ± 0.075 V
- (ERR2, ERR1, ERR0) = (0, 1, 0) = DC-link undervoltage = 0.75 V ± 0.075 V
- (ERR2, ERR1, ERR0) = (0, 1, 1) = Overcurrent = 1.125 V ± 0.075 V
- (ERR2, ERR1, ERR0) = (1, 0, 0) = Overtemperature = 1.5 V ± 0.075 V
- (ERR2, ERR1, ERR0) = (1, 0, 1) = Power supply = 1.875 V ± 0.075 V
- (ERR2, ERR1, ERR0) = (1, 1, 0) = Application = 2.25 V ± 0.075 V
- (ERR2, ERR1, ERR0) = (1, 1, 1) = Manual = 2.625 V ± 0.075 V

In error state PWM pulses are inhibited and Power Stage is not ready for operation. In order to allow PWM pulses and Power Stage operation, controller have to first acknowledge error through Controller Board interface J1-pin 36 (ERR_RST_DSP/GPIO-59).

Alternatively, error can be acknowledged externally by corresponding switch/button connected to dedicated GPIO Board digital input (DIG-IN6, in case of GPIO-01 Board) or by means of software using General Error Reset button in PERUN PowerDesk.

By acknowledging, error is only cleared but PWM pulses are not automatically enabled.

PWM pulses can be enabled/disabled by controller through dedicated Controller Board interface J1-pin 60 (PWM_EN/GPIO-49).

3.3 OVERCURRENT PROTECTION CIRCUIT

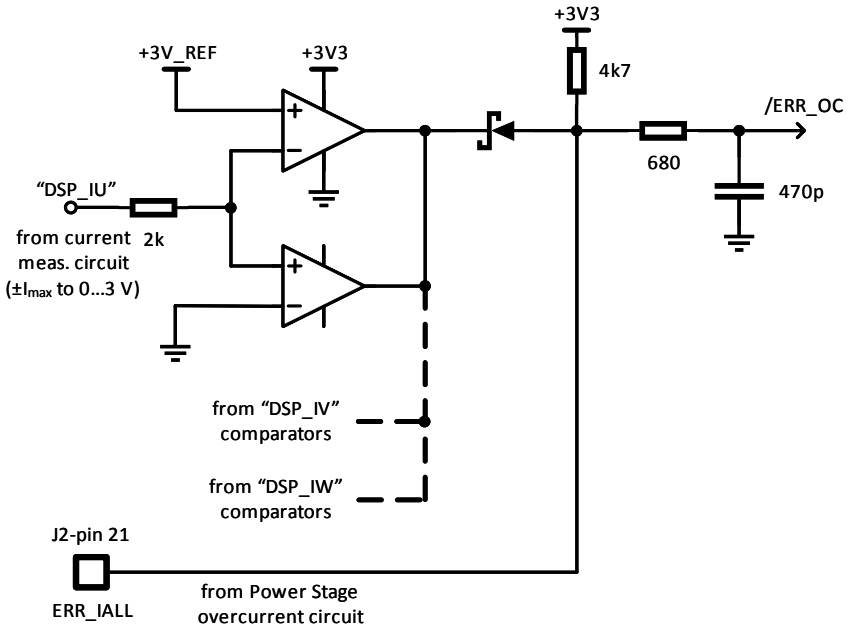


Figure 23: Overcurrent error signal /ERR_OC generation circuit – functional overview

There are two sources of overcurrent error signal:

- Motherboard current comparators.
  - Measured current signals "DSP_IU", "DSP_IV", and "DSP_IW" (conditioned Power Stage inverter output currents which are additionally filtered and connected to corresponding Controller Board analog inputs) are compared with fixed references +3V (upper limit) and 0 V (lower limit) to detect overcurrent values. Absolute overcurrent values (in Amps) depend on current measurement circuit gains. By default, gains are set to trigger overcurrent error signal for actual current values above ±2.5 times higher than Power Stage nominal output current amplitude. However, different current measurement range and overcurrent limits can be specified during purchasing process.

- Power Stage output current comparators.
  - Power Stage integrates overcurrent detection circuit and provides digital error signal on J2-pin 21 (ERR_IALL). This signal is OR'ed with open-colector outputs of current comparators on Motherboard, to generate final overcurrent error signal /ERR_OC. PERUN Power Stage overcurrent limits are fixed and determined according to the integrated semiconductors current rating, in order to maintain its safe operation. Overcurrent limits are set to values ±2.5 times higher than Power Stage nominal output current amplitude.

- Example: for considered 5.5 kW industrial converter, nominal inverter output current value is 12 Arms. Nominal current amplitude is 1.41 x 12 = 16.92 A. Therefore, fixed overcurrent limit values are ±2.5 x 16.92 A = 42.3 A. This value assures safe operation of Power Stage. However, user can specify Motherboard current measurement gains in order to react on lower overcurrent values (to properly protect lower power loads/sources). User has to simply look on this feature as two-level overcurrent protection system.

3.4 DC-LINK UNDER/OVERVOLTAGE PROTECTION CIRCUIT

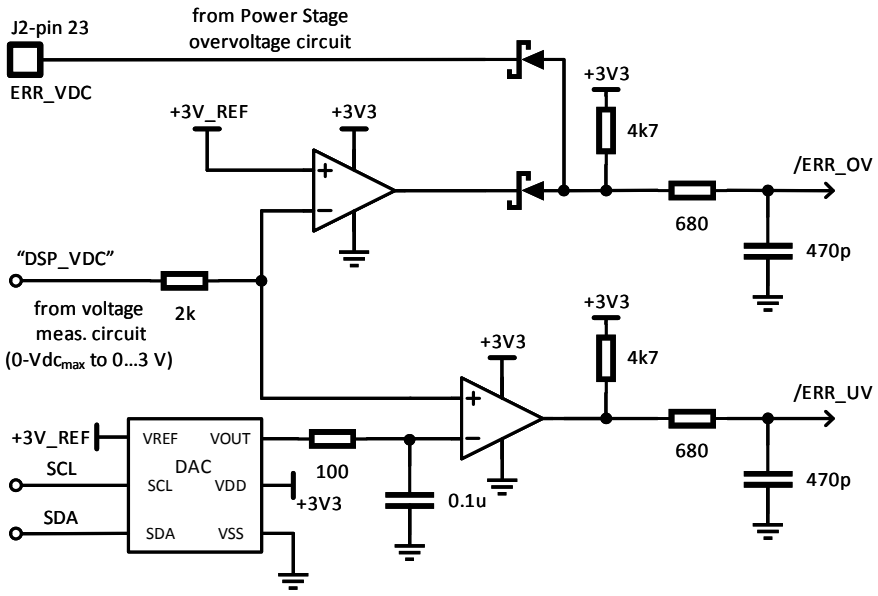


Figure 24: DC-link undervoltage (/ERR_UV) and overvoltage error signal (/ERR_OV) generation circuit – functional overview

There are two sources of DC-link overvoltage error signal (/ERR_OV):

- Motherboard DC-link overvoltage comparator.
  - Measured DC-link voltage signal "DSP_VDC" (conditioned Power Stage DC-link voltage which is additionally filtered and connected to corresponding analog input) is compared with fixed reference voltage +3V (+3V_REF) to detect overvoltage value. Absolute overvoltage value (in Volts at Power Stage DC-link) depends on DC-link voltage measurement circuit gain. By default, gain is set to trigger overvoltage error signal for actual DC-link voltage above 790 V. However, different DC-link voltage measurement range and overvoltage limit can be specified during purchasing process. This feature can be helpful for more precise measurement and protection in low voltage applications (e.g. when DC-link voltage is below 300 V).

- Power Stage DC-link overvoltage comparator.
  - Power Stage integrates DC-link overvoltage detection circuit and provides digital error signal on J2-pin 23 (ERR_VDC). This signal is OR'ed with open-colector output of DC-link overvoltage comparator on Motherboard, to generate final overvoltage error signal /ERR_OV. Power Stage DC-link overvoltage limit is fixed and determined according to the maximum voltage rating, in order to maintain its safe operation. DC-link overvoltage limit is set to 790 V.

DC-link undervoltage error signal /ERR_UV is generated by comparing measured DC-link voltage signal “DSP_VDC” (see section “DC-link voltage measurement circuit”) and reference undervoltage limit defined at integrated DAC (digital-to-analog) circuit output. By default, actual (Power Stage) DC-link undervoltage limit is set to 300 V, but different value can be specified in purchasing process. Additionally, using specialized PERUN PowerDesk software component user can set desired undervoltage limit.

3.5 MANUAL ERROR TRIGGER CIRCUIT

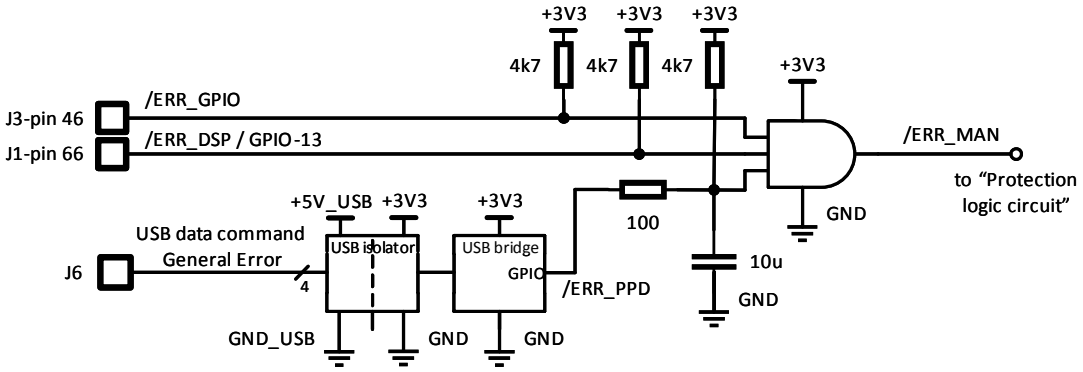


Figure 25: Manual error trigger circuit – functional overview

There are three sources of manual error signal (/ERR_MAN):

- /ERR_GPIO – GPIO Board external error input. Every GPIO Board has dedicated digital input for error triggering. For example, user can connect Emergency Stop button at this input. User input (on GPIO board) is isolated and conditioned to +3.3 V level of /ERR_GPIO signal at GPIO board interface J3-pin 46. Signal is active low.

- /ERR_DSP/GPIO-13 - Controller Board dedicated output. Controller Board interface J1-pin 66 (/ERR_DSP/GPIO-13) is dedicated for triggering of manual error. In this way, user can implement various kinds and levels of protection through control code. It is suggested that user implement software protections (overcurrent, overload, under/overvoltage, overtemperature, etc.) with limit values which are below described hardware implemented errors. Signal is active low.

- PERUN PowerDesk (PPD) General Error button. PPD has dedicated button "General Error" for triggering of manual error. By activating the button, corresponding command is sent over J6 USB interface to integrated USB/UART (/JTAG/I2C/GPIO) bridge which controls /ERR_PPD signal state. Once the General Error button is pressed, signal /ERR_PPD is low for cca. 1 second, which will trigger /ERR_MAN and /ERR error signals. At /ERR_PPD line one can notice RC circuit which is forcing /ERR_MAN error active (and complete error signal /ERR) during power-up process. Due to this feature, initial Power Stage state is error state where PWM pulses are inhibited. In order to enable Power Stage operation user has to clear/acknowledge the error.

3.6 ERROR SIGNAL RESET CIRCUIT

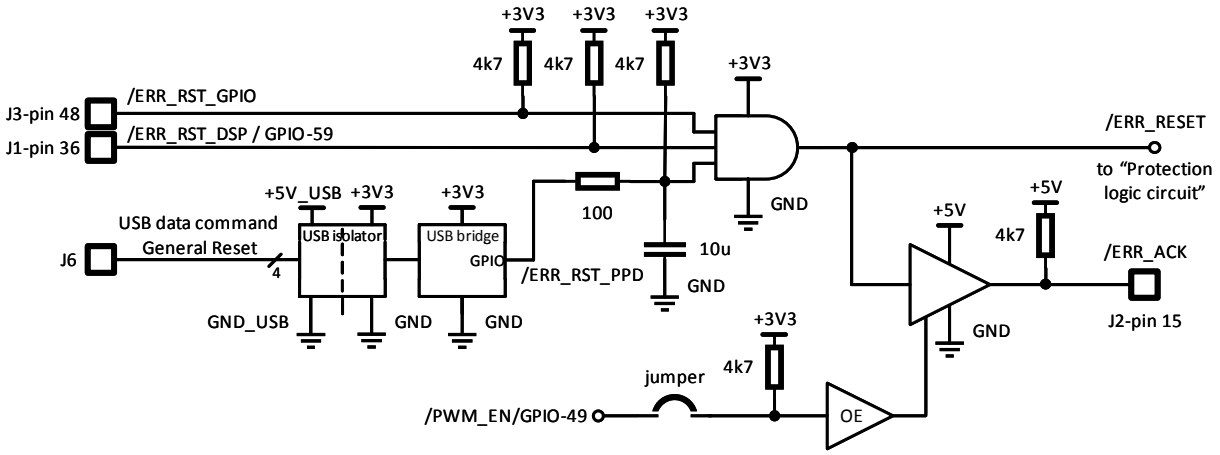


Figure 26: Error reset circuit – functional overview

There are three sources of error reset signal (/ERR_RESET) for clearing LARA-100 system error state:

- /ERR_RST_GPIO - GPIO Board external error reset input. Every GPIO Board has dedicated digital input for resetting LARA-100 system error state. For example, user can connect error reset button at this input. User input (on GPIO board) is isolated and conditioned to +3.3 V level of /ERR_RST_GPIO signal at GPIO board interface J3-pin 48. Signal is active low.

- /ERR_RST_DSP/GPIO-59 - Controller Board dedicated output. Controller Board interface J1-pin 36 (/ERR_RST_DSP/GPIO-59) is dedicated for error acknowledgment. In this way, user can implement error acknowledgment procedure through control code. Signal is active low.

- PERUN PowerDesk (PPD) General Reset button. PowerDesk has dedicated button "General Reset" for resetting LARA-100 system error reset (also, Capture/Scope communication with controller is put in initial state). By activating the button, corresponding command is sent over J6 USB interface to integrated USB/UART (/JTAG/I2C/GPIO) bridge which controls /ERR_RST_PPD signal state. Once the General Reset button is pressed, signal /ERR_RST_PPD is low for cca. 1 second, which will put /ERR_RESET signal in active state.

/ERR_RESET signal is main error reset signal on Motherboard. Its state is also reflected at Power Stage interface J2-pin 15 (/ERR_ACK) dedicated for acknowledgment error signal on Power Stage. Voltage translator is used for buffering +3.3 V /ERR_RESET signal to +5 V /ERR_ACK signal which is provided to Power Stage. By default, controller pulse enable /PWM_EN/GPIO-49 signal determine if the Power Stage error can be cleared or not. If /PWM_EN signal is active (low) and PWM pulses are enabled, /ERR_ACK signal will remain inactive (high +5V) independently on /ERR_RESET signal state. This feature provides additional safety measure of PERUN Power Stage SiC Mosfet drivers. This is why user have to firstly assure, through control code, that PWM pulses are disabled (/PWM_EN inactive) and then to clear an error (/ERR_ACK active).

3.7 PWM PULSES ENABLE CIRCUIT

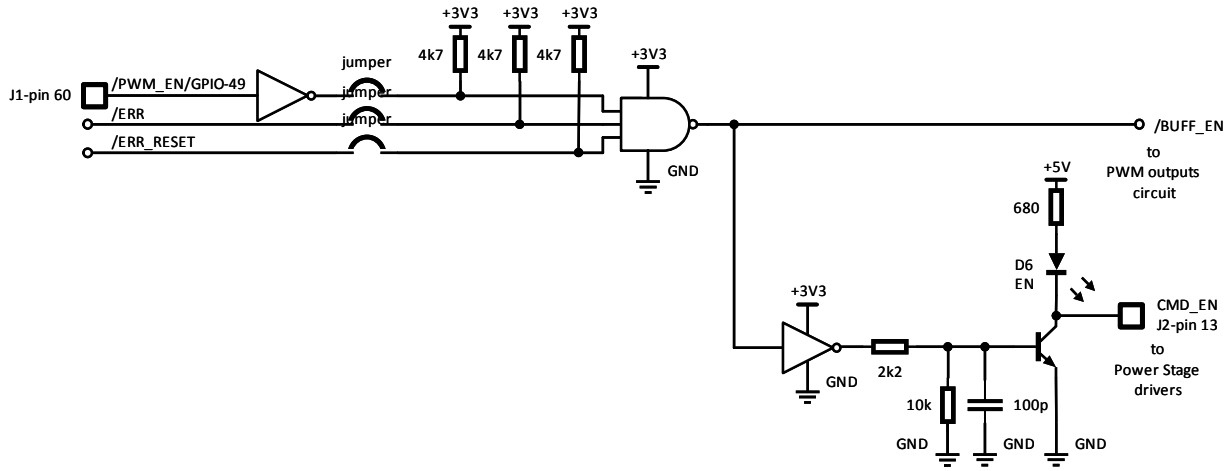


Figure 27: PWM pulses enable circuit – functional overview

PWM pulses are inhibited if one of the following situations:

- /PWM_EN/GPIO-49 – Controller dedicated output for PWM enable/disable. If /PWM_EN is inactive (high +3.3V), /BUFF_EN signal which is routed to enable input of PWM outputs circuit (PWM buffer) will be also inactive. Signal is also translated to +5 V level signal CMD_EN at Power Stage interface J2-pin 13, which will inhibit operation of PERUN Power Stage SiC Mosfet drivers. Green LED D6 (EN – Enable PWM operation) is switched off, indicating that PWM pulses and IGBT drivers are disabled.
- /ERR – Global error signal (see section “Protection circuits”). In error state, when /ERR signal is active (low 0 V), /BUFF_EN and CMD_EN signals will be in inactive state. /BUFF_EN inhibits PWM pulses on Motherboard level, and CMD_EN inhibits PWM pulses on PERUN Power Stage level and puts SiC Mosfet gate drive signals in safe inactive state.
- /ERR_RESET – Global error reset signal (see section “Error protection circuit”). If there is an error acknowledgment in progress and /ERR_RESET signal is active (low 0 V), /BUFF_EN and CMD_EN signals will be in inactive state, and PWM pulses will be disabled. This feature is introduced as safety measure of PERUN Power Stage SiC Mosfet drivers. Using this logic, it is impossible to damage Power Stage output due to situation where controller generates PWM pulses and /ERR_RESET is active.

In other words, PWM pulses are enabled and provided to Power Stage only if all following statements are satisfied:

- There is no active error. /ERR signal is inactive high (+3.3 V).
- There is no active error acknowledgment in progress. /ERR_RESET is inactive high (+3.3 V).
- Controller (user control code) generates active low PWM enable signal /PWM_EN at Controller Board interface J1-pin 60.

Enabled PWM operation is indicated with green LED D6 (EN) switched-on.

3.8 CURRENT MEASUREMENT CIRCUIT

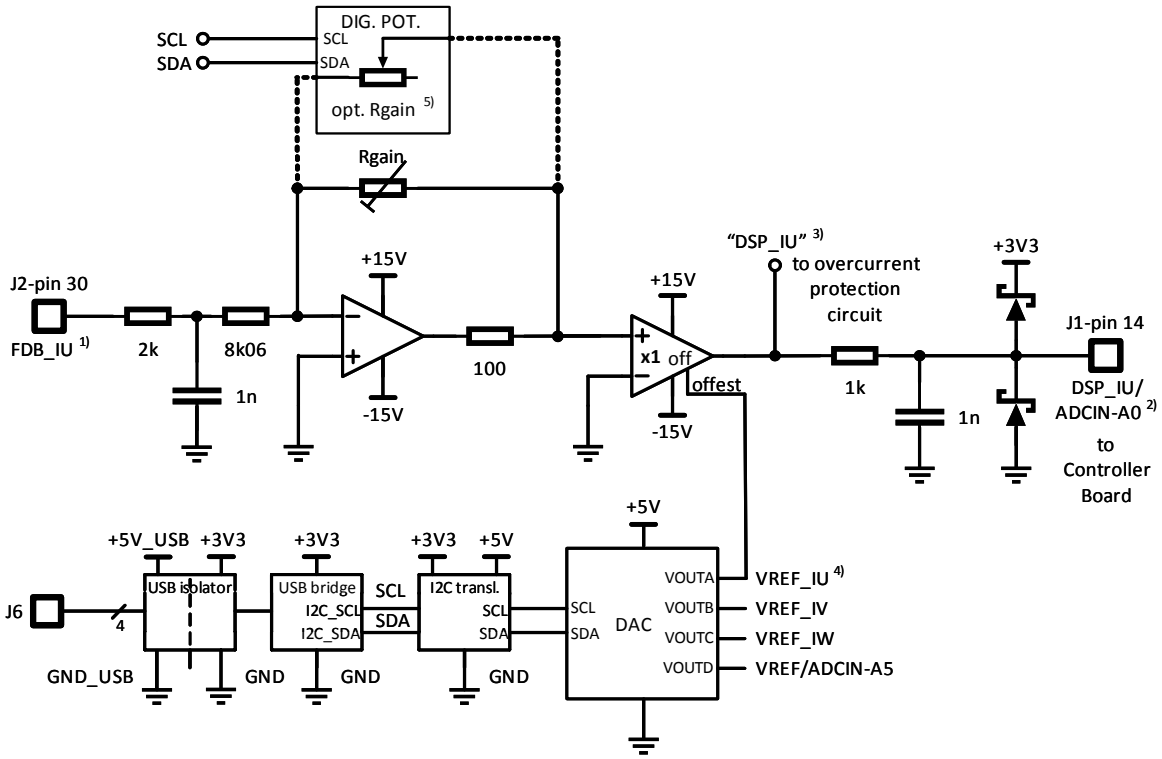


Figure 28: Current measurement circuit (shown for phase U current - IU) – functional overview

1) For all inverter output currents IU, IV, and IW there are an identical measurement circuit on LARA-100 Motherboard. Instead J2-pin 30 FDB_IU feedback signal from Power Stage, for other two currents there are:

- J2-pin 28 FDB_IV signal
- J2-pin 26 FDB_IW signal

2) Instead measured current DSP_IU signal at Controller Board interface J1-pin 14 (at controller analog input ADCIN-A0), for other two currents there are:

- measured current signal DSP_IV at Controller Board interface J1-pin 18 (at ADCIN-A1 analog input)
- measured current signal DSP_IW at Controller Board interface J1-pin 22 (at ADCIN-A2 analog input)

3) "DSP_IU", "DSP_IV", and "DSP_IW" are measured inverter output current signals which are compared with set current limit values in Protection circuit for detecting overcurrent error states (see section "Overcurrent protection circuit").

4) VREF_IU, VREF_IV, and VREF_IW are offset values for measured inverter output currents IU, IV, and IW. By default, offset voltage values VREF_IU, VREF_IV and VREF_IW are pre-set to 1.5 V. This situation

is suitable for AC applications, where measured current values DSP_IU, DSP_IV, and DSP_IW are conditioned to 0-3 V voltage range (at controller analog inputs) around 1.5 V offset. This means, if actual current value IU is 0 A, measured current signal DSP_IU will be 1.5 V. For positive current values measured voltage representative is above 1.5 V (from 1.5 to 3 V), and for negative current values measured signal is below 1.5 V (from 1.5 to 0 V). For DC applications, such as Boost/Buck converters, it may be suitable to set offset values near 0 V (e.g. 0.2 V) or 3 V (e.g. 2.8 V) to extend measuring range and maintain highest possible measuring resolution. Different offset value can be specified in purchasing process. Additionally, using specialized PERUN PowerDesk software component for LARA-100 system configuration, user can set desired offset value. Set offset value VREF is also provided to the controller through analog input ADCIN-A5 which can be used for offset adjustments in user control code.

[5)] Current measurement gains are fixed in manufacturing process according to user demands, with pre-set resistor Rgain. For future use, there is an optional digital potentiometer in current measurement circuit feedback path which can be set by using specialized PPD configuration software component. Using this feature, user can set desired current measurement gains (and current range/limits by that way) and fully adapt the same LARA-100 system to different loads/sources. However, this feature is not available in LARA-100 Motherboard v1.3 revision.

Current measurement gains and offset values are pre-set during manufacturing process of LARA-100 Motherboard, and according to user specification. If not specified, gains are set to transfer actual current range from -2.5*In_amp to +2.5*In_amp, to 0-3 V range at controller analog inputs, with 1.5 V offset value (where In_amp represent nominal amplitude of inverter output current).

For example, for considered industrial 5.5kW converter, nominal output current is 12 Arms. In this case, current range from -42.3 A to +42.3 A (2.5*1.41*12 = 42.3 A) will be transferred to voltage range 0-3 V, with 1.5 V offset value (0 A → 1.5 V). Measuring current range -2.5*In_amp to +2.5*In_amp assures full utilization of converter power at nominal voltage, and at the same time safe operation where overload and overcurrent situations can be detected without damaging Power Stage. It is only allowed to reduce current measurement range (by specifying Rgain) compared to default ±2.5*In_amp range.

3.9 DC-LINK VOLTAGE MEASUREMENT CIRCUIT

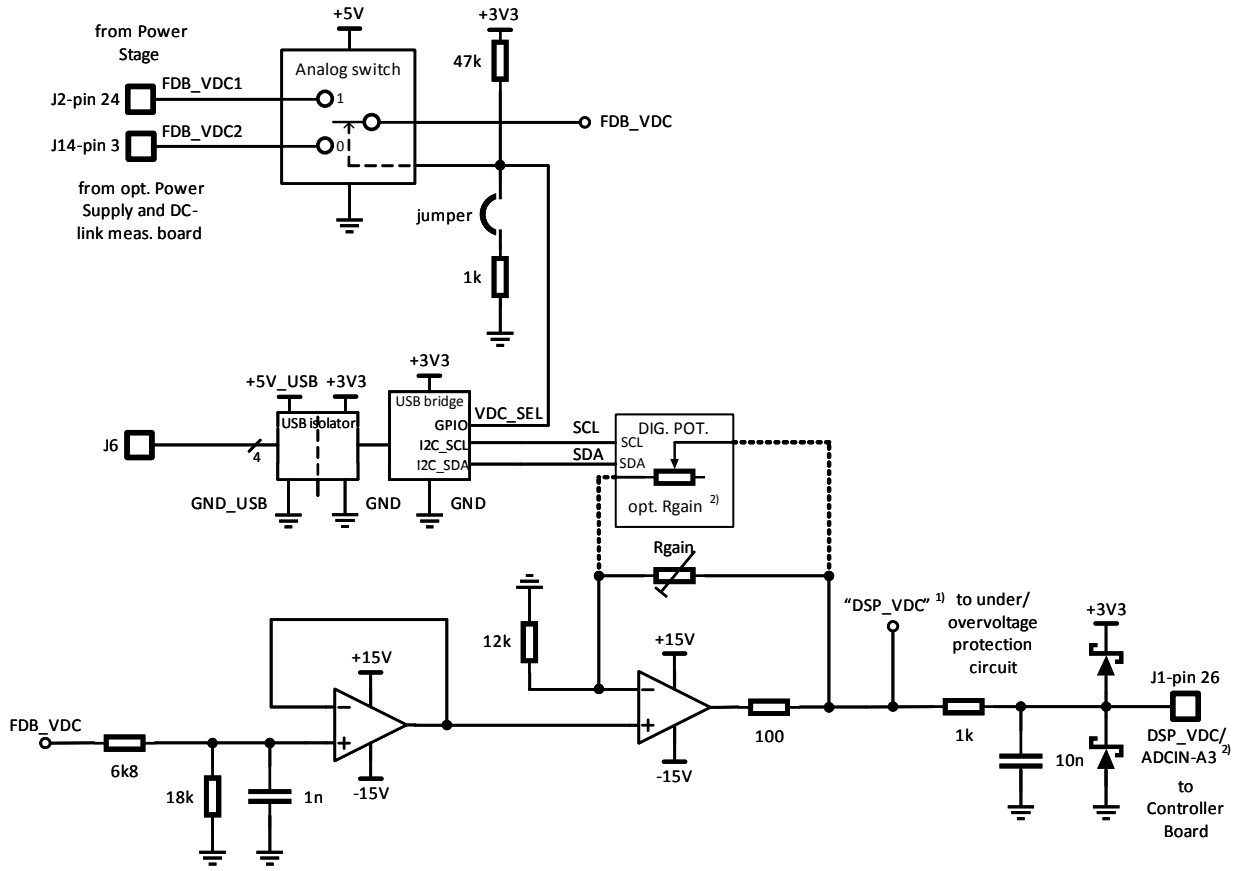


Figure 29: DC-link voltage measurement circuit – functional overview

1) "DSP_VDC" is measured DC-link voltage signal which is compared with set voltage limit values in Protection circuit section for detecting under/overvoltage error states (see section DC-link under/overvoltage protection circuit).

2) DC-link voltage measurement gain is fixed in manufacturing process according to user demands, with pre-set resistor Rgain. For future use, there is an optional digital potentiometer in voltage measurement circuit feedback path which can be set by using specialized PERUN PowerDesk configuration software component. Using this feature, user will be able to set desired voltage measurement gain (and DC-link voltage limits by that way) and fully adapt the same LARA-100 system to different voltage levels (i.e. to low and high voltage applications, from 48 V to 800 V DC-link voltage). However, this feature is not available in LARA-100 Motherboard v1.3 revision.

Voltage measurement gain value is pre-set (by Rgain) during manufacturing process of LARA-100 Motherboard, and according to user specification. If not specified, gain is set to transfer actual DC-link voltage range from 0 to 800 V, to 0-3 V range at controller analog input (without offset value). Default measurement gain is equal to 3 V / 800 Vdc = 0.00375 V/Vdc.

Source of measured DC-link voltage can be selected, either by removing/placing corresponding jumper on Motherboard or by using specialized PERUN PowerDesk configuration software component. Power Supply board, used within Power Stage, is provided with measured DC-link voltage feedback signal at Power Stage interface J2-pin 24 (FDB_VDC1) correctly represent actual DC-link voltages from 200 V to 800 V. In that way it represents suitable solution for applications where DC-link voltage is above 300 V. For low voltage applications, user has to consider use of PERUN's LARA-100 optional Power Supply and DC-link Measurement Board which properly operates with lower DC-link voltages and extends measurement range of actual DC-link voltage up to 0 V. In this case, user has to select input DC-link signal FDB_VDC2 at interface J14-pin 3, by placing corresponding jumper in VDC selection circuit or by specifying this selection in PPD software suite during online connection with LARA-100 system.

3.10 PRE-CHARGE THYRISTOR AND BRAKING CHOPPER TURN ON/OFF CIRCUIT

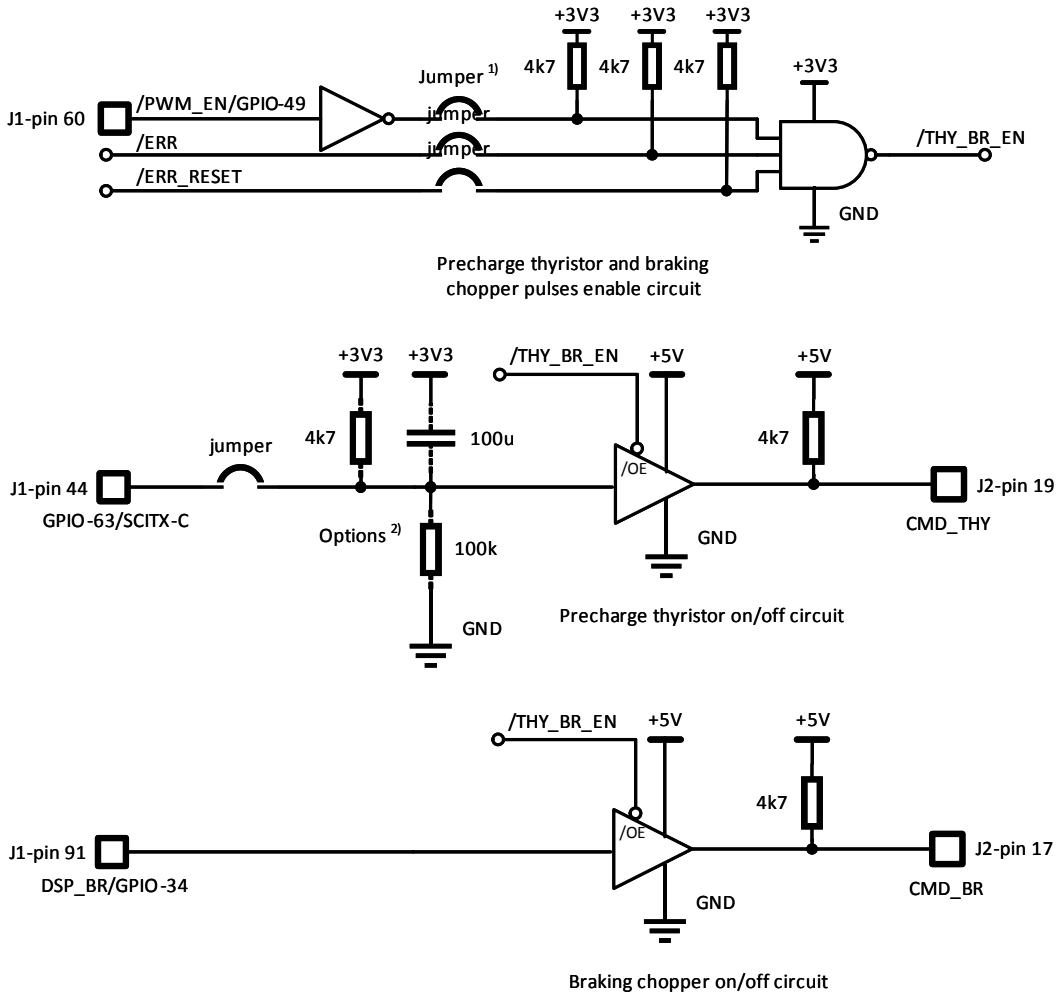


Figure 30: Pre-charge thyristor and braking chopper on/off circuit – functional overview

[1] Pre-charge thyristor and braking chopper pulses enable circuit is independent on PWM pulses enable circuit, and can be set independently. By default, all designated jumpers are placed, so this circuit behaves same as PWM pulse enable circuit (see section "PWM pulses enable circuit"). Briefly, there must not be active error (/ERR), neither error acknowledgment (/ERR_RESET) must not be in progress, and /PWM_EN controller signal must be active. However, user can specify different behavior during purchasing process. For example, user can exclude jumper from /ERR line, if it is desired to control braking chopper even in error state (e.g. in DC-link overvoltage situation, when it is desirable to dissipate power charging DC capacitors).

[2] There are different options for controlling pre-charge thyristor. Possible options, which can be specified during purchasing process, are:

- Regular control – Pre-charge thyrsitor is turned-off during power-up process for defined time interval. Time interval is defined by integrated RC circuit, and it equals up to 5 seconds. After time delay elapses, pre-charge thyristor is automatically turned-on and stays in that state until power is removed from LARA-100 system.
- Controller Board control – Pre-charge thyrsitor can be managed by implemented control code through Controller Board interface J1-pin 44 GPIO-63 signal. In this case, above mention RC delay circuit is not soldered, and controller GPIO-63 pin is connected by jumper to on/off circuit and pulled-up with 4k7 resistor assuring inactive initial state. GPIO-63 turn on/off signal is active low (0 V = on; +3.3 V = off).
- Permanently turned-off – In some applications, there is no requirement for turning on pre-charge thyristor. Examples are applications where DC source or load is directly connected to Power Stage DC-link without using input diode rectifier. In these situations, it is suitable that pre-charge thyristor is permanently turned-off. It can be done by removing GPIO-63 line jumper and placing pull-up resistor 4k7 at the input.

3.11 COMMUNICATION CIRCUITS

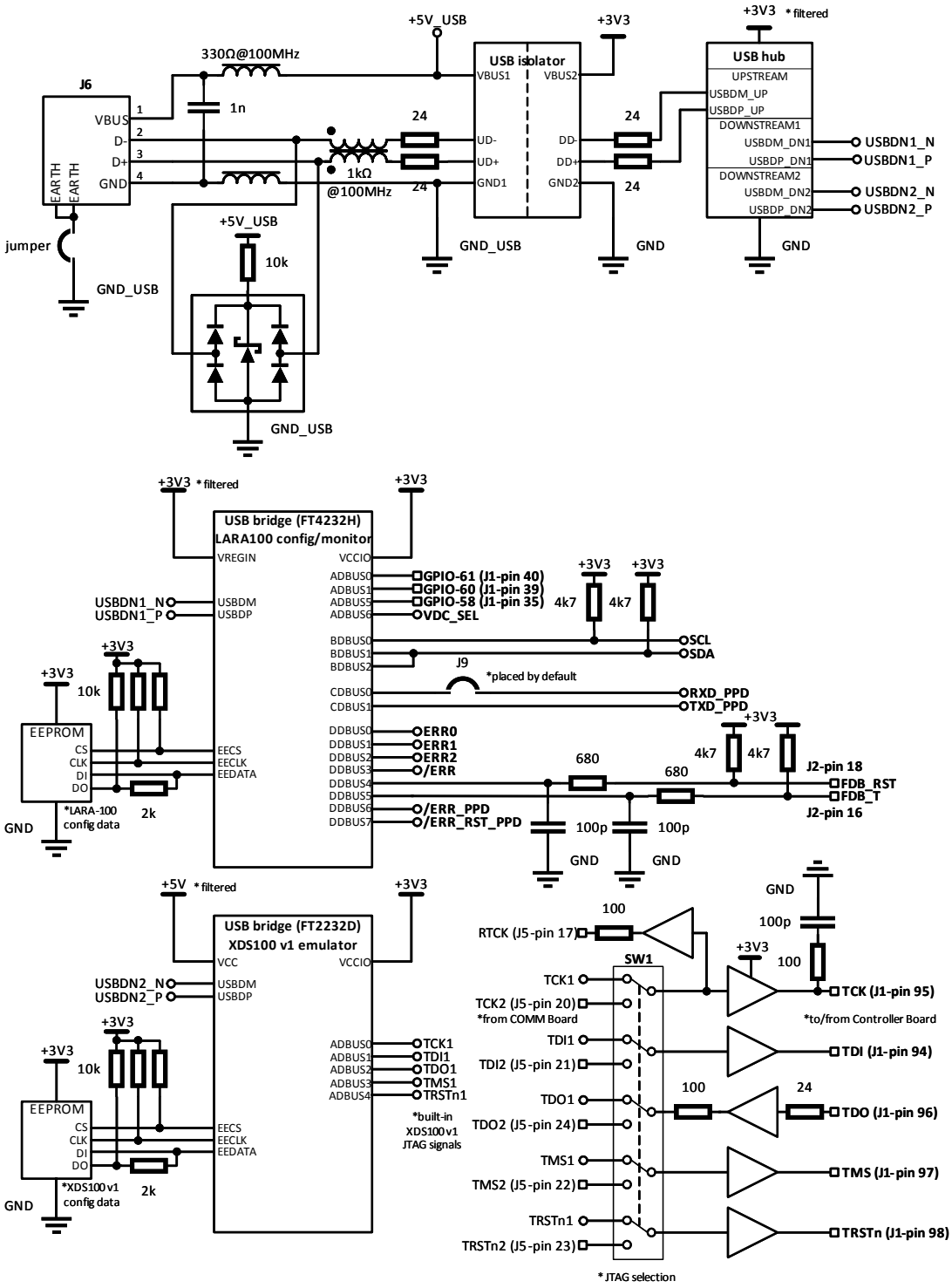


Figure 31: Communication circuits – functional overview

J6 USB interface is used for communication between PERUN PowerDesk software suite and complete LARA-100 system. For this purpose LARA-100 Motherboard integrates communication circuits, which functional schematic diagram is shown in previous figure. USB interface is isolated and then separated in two main parts:

- LARA-100 config/monitor circuit – This part is used for configuration of programmable features on Motherboard and Expansion Boards (GPIO, APP, and COMM), for monitoring and control of LARA-100 system operational states, and for communication between PERUN PowerDesk and Controller Board for the purpose of higher-level control, monitor and control code debugging.
- On-board XDS100 v1 JTAG emulator – This part can be used for programming Controller Board through JTAG communication interface and for control code low-level debugging. It provides interface to standard manufacturer's Integrated Development Environments (such as CCS – Code Composer Studio for Texas Instruments microcontrollers), even it can be used directly with PERUN PowerDesk (e.g. for downloading control code).

PERUN PowerDesk (PPD) software is using J6 USB interface for monitoring and control of LARA-100 system operational states. GPIO interface of integrated USB bridge circuit (FT4232H) is used for this purpose. PPD cyclically reads global error signal /ERR and error code signals ERR2, ERR1 and ERR0 which indicates operational and error states of LARA-100 system. In PPD user can interconnect these signals with arbitrarily defined error messages and actions.

PPD can trigger error through /ERR_PPD signal. Clicking on the PPD "General Error" button generates active low /ERR_PPD signal. Once it is activated /ERR_PPD signal is low for cca. 1 second, and automatically gets back to inactive high state. Similarly, error acknowledgment can be done using PPD "General Reset" button which generates active low /ERR_RST_PPD signal. Once it is activated /ERR_RST_PPD signal is low for cca. 1 second, and automatically gets back to inactive high state.

PPD cyclically reads Power Stage feedback signals FDB_RST and FDB_T for monitoring power supply at input terminals of integrated three-phase diode rectifier. In this way, PPD can automatically check if user had connected power supply at diode rectifier inputs, and if the connected source is three-phase or single-phase type. In this way, PPD can generate warning and alarm messages in situations when defined project properties (LARA-100 application data) do not match actual application of considered LARA-100 system. This feature additionally protects system against possible damage.

Instead of using hardware way of defining feedback source for measured DC-link voltage, user can take advantage of PPD for selection between J2 interface and J14 interface DC-link voltage feedback signal (see section "DC-link voltage measurement circuit"). PPD is controlling VDC_SEL signal for this purpose.

PPD controls SDA and SCL signals for communication with programmable circuits on Motherboard and Expansion Boards (GPIO, APP, and COMM Boards). In this way, user can configure certain LARA-100 system programmable features according to requirements, by using specialized PPD configuration software component. Motherboard v1.3 has following features which can be configured through PPD:

- Offset values for current measurement circuits (see section “Current measurement circuit)
- DC-link undervoltage limit value (see section DC-link under/overvoltage protection circuit)
- Programmable current measurement gains and DC-link voltage measurement gain (range/limits) are reserved for future use (revisions above v1.3)

PPD uses integrated USB/UART bridge on Motherboard as main communication path with Controller Board. Motherboard signals RXD_PPD and TXD_PPD, are connected to Controller Board pins dedicated for UART (SCI) communication (controller UART/SCI peripheral pins RX and TX). By integrating pre-prepared PPD library and functions into the control code and reserving part of controller’s memory and UART/SCI peripheral, user can read and manipulate any defined variable from control code in user-friendly manner using PPD software suite.

All Motherboard’s configuration data which are pre-set during manufacturing process (factory settings) are stored on the EEPROM memory belonging to LARA-100 config/monitor USB bridge circuit. PPD uses the EEPROM data for automatic detection and validation of LARA-100 Motherboard.

With LARA-100 system user can select between two possible JTAG communication paths with Controller Board. First option is using on-board XDS100 v1 JTAG emulator, and second option is using J5 Communication Board JTAG interface together with external JTAG programmer/debugger. Motherboard switch SW1 is used for selection. By default, Motherboard comes with a setting which connects on-board XDS100 JTAG emulator to Controller Board JTAG pins. Control code can be downloaded through PPD or manufacturer’s Integrated Development Environment (e.g. CCS for TI controllers). However, if user has appropriate Communication Board with implemented JTAG interface (e.g. PERUN’s COMM-01 and COMM-02 Boards) and want to use external JTAG programmer/debugger, he have to put SW1 switch in opposite position (designated on the Motherboard).

3.12 POWER SUPPLY CIRCUITS

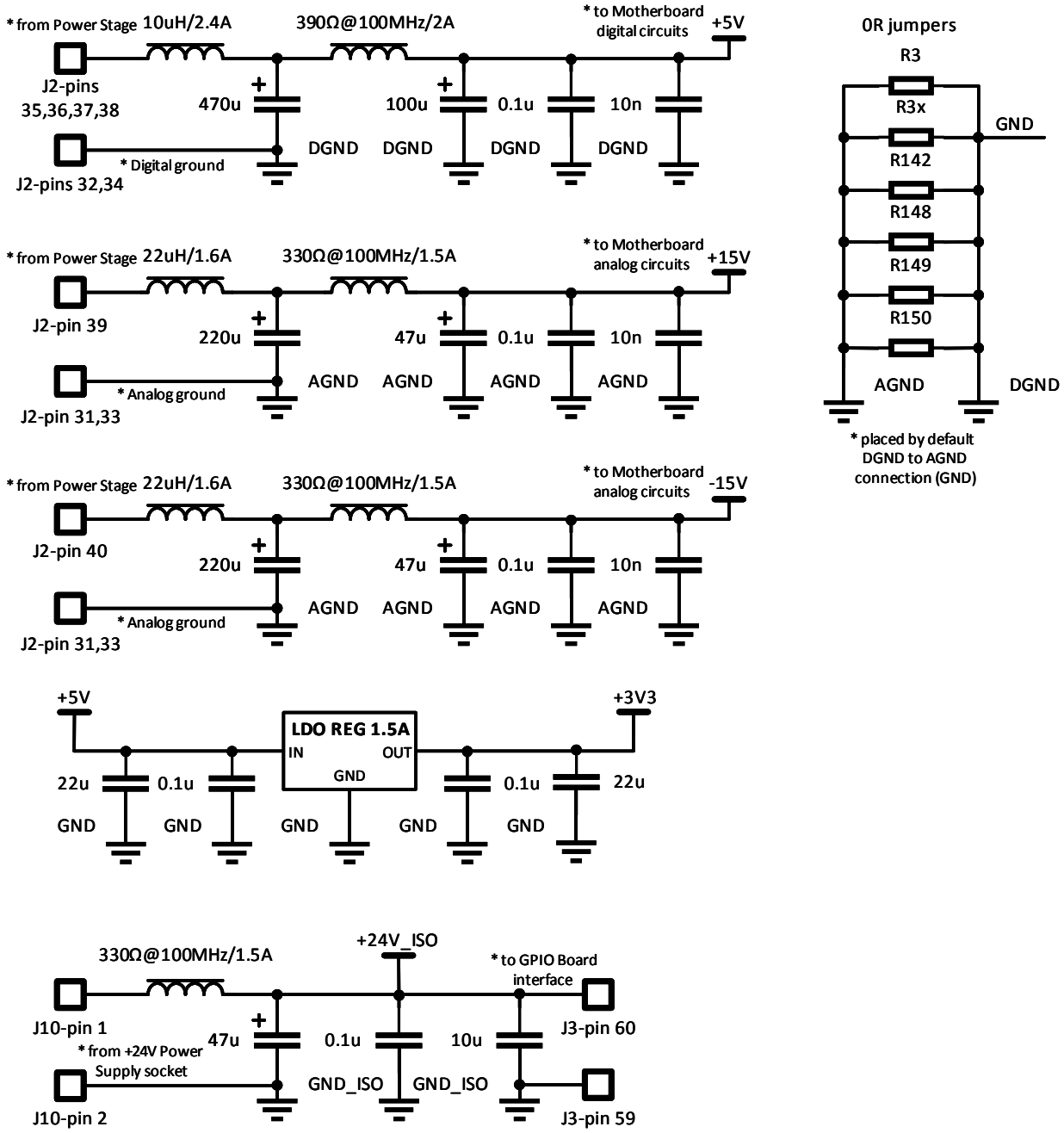


Figure 32: Power Supply circuits – functional overview

Note

Digital (DGND) and analog ground planes (AGND) on Motherboard are routed separately to assure less interference between digital and analog circuits. Special care is done in PCB design to provide good quality of analog feedback (measurement) signals with reduced noise. However, by default they are connected at appropriate positions making unique ground reference GND. Ground reference (GND) is designated in all previous functional schematics, even if AGND is actually used for on-board analog circuits and DGND for digital circuits.

4 CONNECTION EXAMPLES

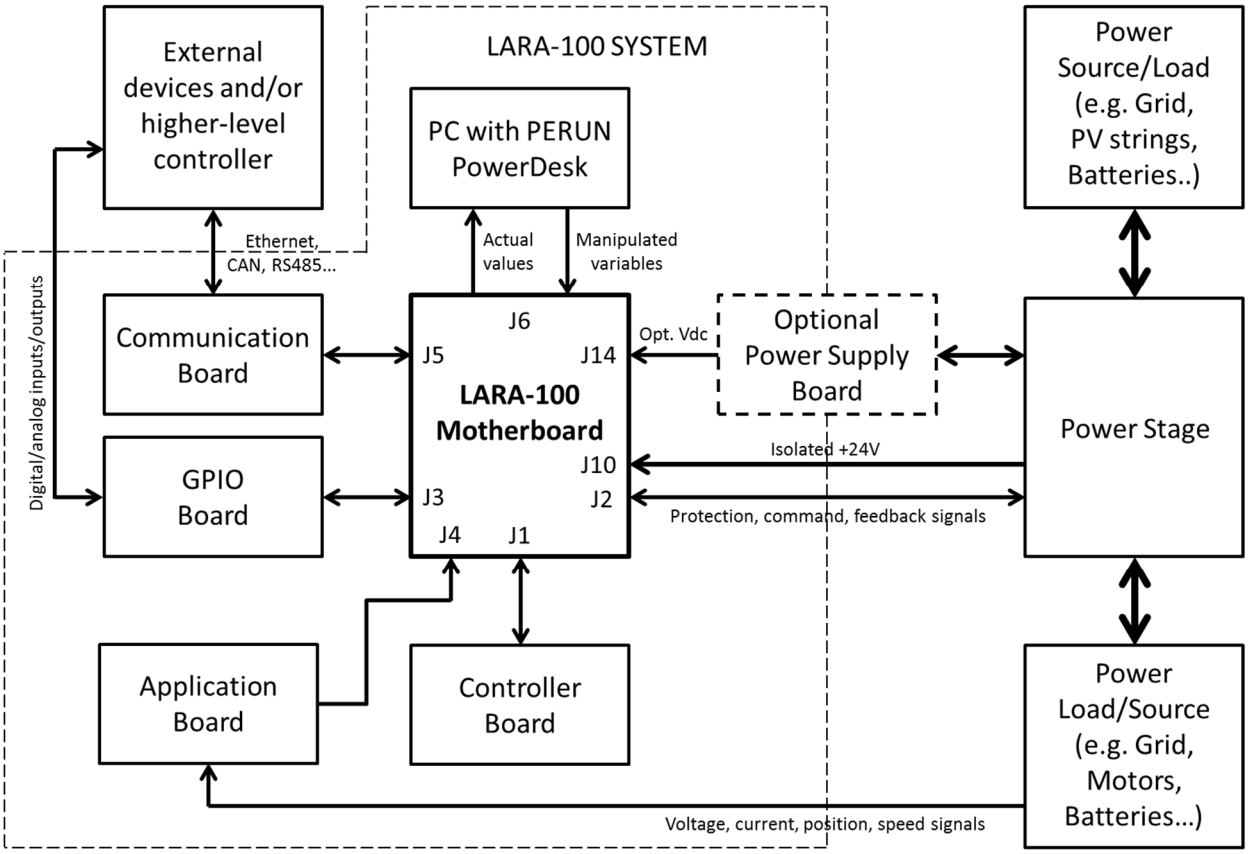


Figure 33: Schematic structure of LARA-100 system – general overview of connections between Motherboard and other components

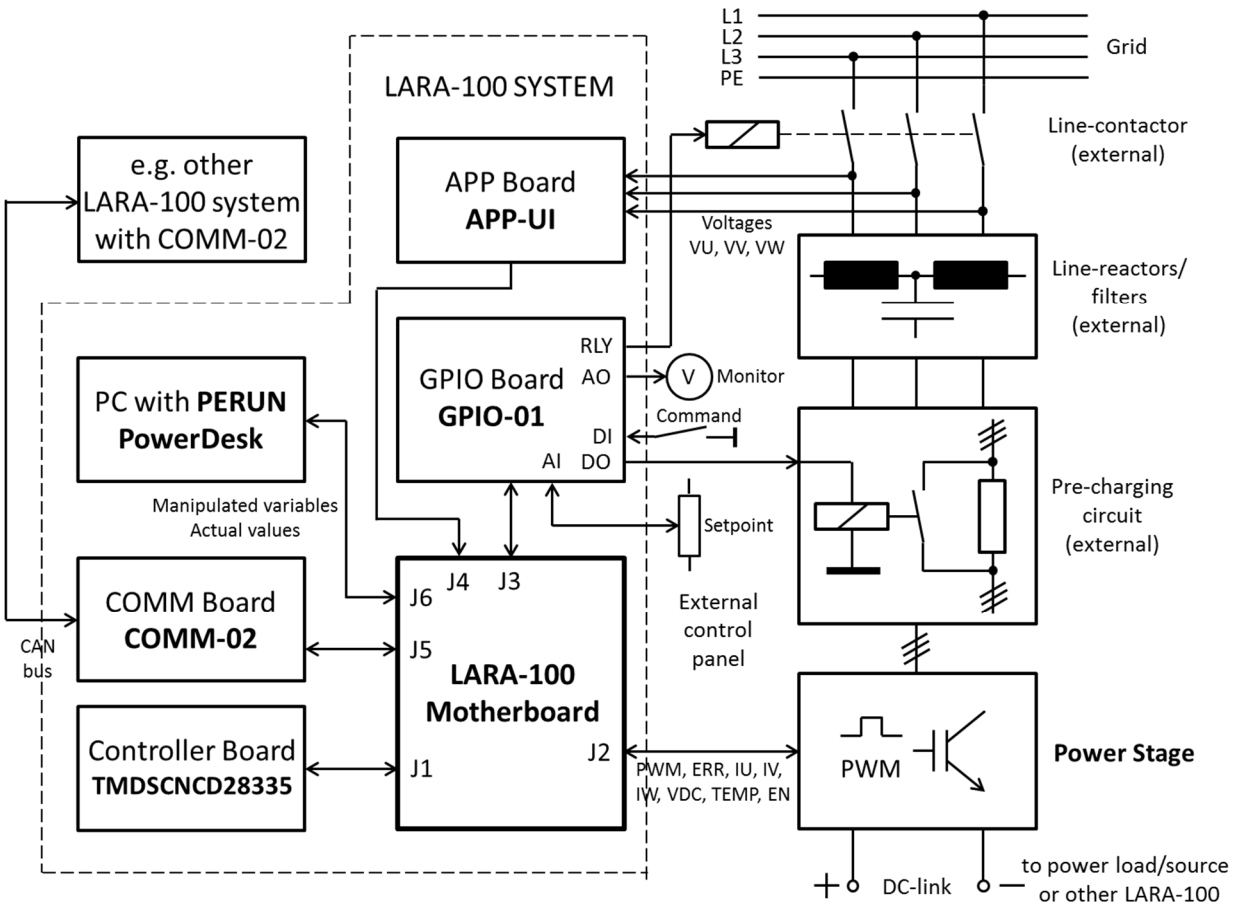


Figure 34: Schematic structure of LARA-100 grid-connected converter system - LARA-100 GCC

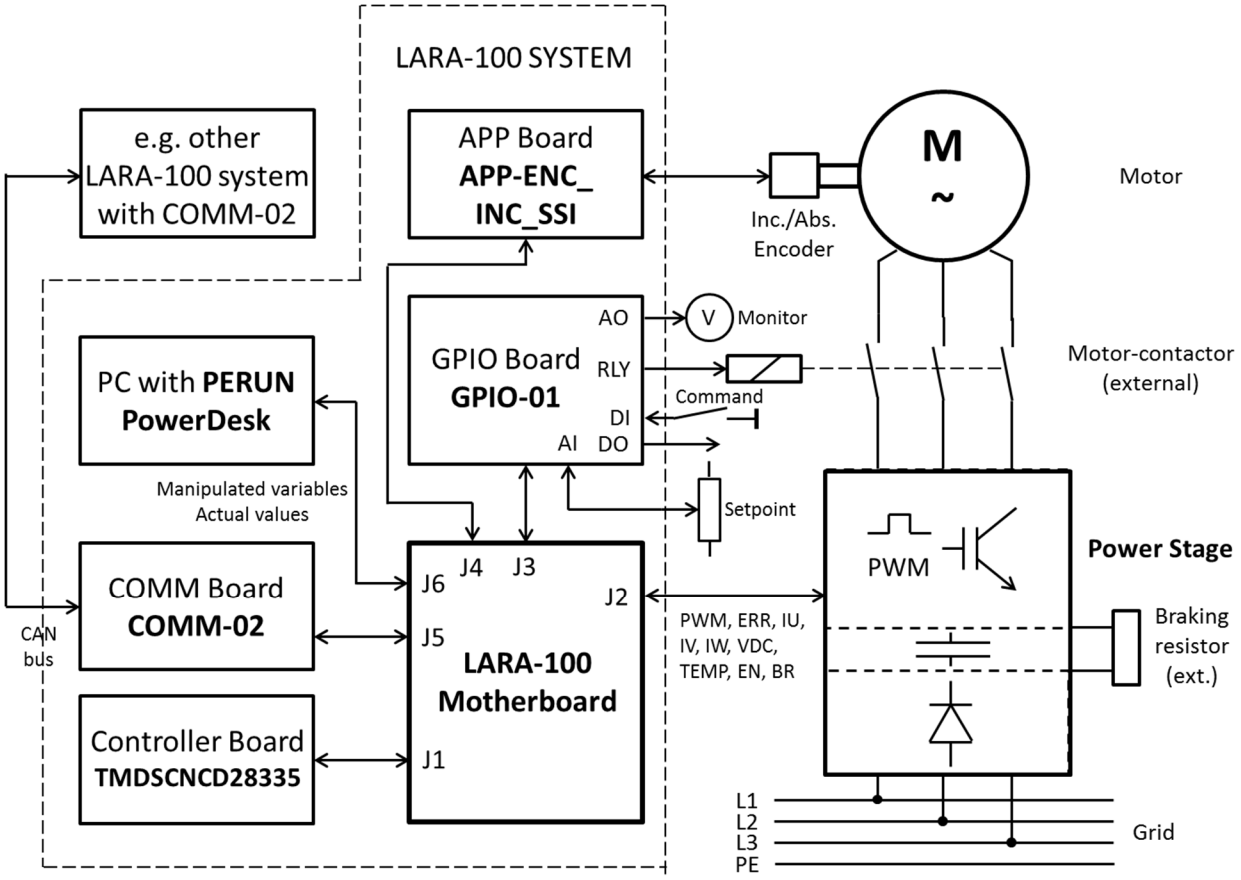


Figure 35: Schematic structure of LARA-100 motor drive system - LARA-100 MD

5 DOCUMENT HISTORY

Date	Version	Responsible person	Revision details
2017-03-09	1.0		
2019-12-15	1.1	Zoran Relić	Adapted accordingly to the new Power Stage.
2019-12-24	1.2	Zoran Relić	Publicly released